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Optimized ONO thickness for multi-level and 2-bit/cell operation for wrapped-select-gate (WSG) SONOS memory

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Abstract

In this paper, highly reliable wrapped-select-gate (WSG) silicon–oxide–nitride–oxide–silicon (SONOS) memory cells with multi-level and 2-bit/cell operation have been successfully demonstrated. The source-side injection mechanism for WSG-SONOS memory with different ONO thickness was thoroughly investigated. The different programming efficiencies of the WSG-SONOS memory under different ONO thicknesses are explained by the lateral electrical field extracted from the simulation results. Furthermore, multi-level storage is easily obtained, and good V_{TH} distribution presented, for the WSG-SONOS memory with optimized ONO thickness. High program/erase speed (10 μs/5 ms) and low programming current (3.5 μA) are used to achieve the multi-level operation with tolerable gate and drain disturbance, negligible second-bit effect, excellent data retention and good endurance performance.

1. Introduction

According to the International Technology Roadmap for Semiconductors [1], aggressively scaling the traditional floating-gate flash EEPROM device below 70 nm node technology faces numerous challenges, including serious short-channel effects, obvious gate injection, large stress-induced leakage current [2] and critical floating gate (FG) to floating gate coupling [3]. Of all the limiting factors, the most serious one is the oxide leakage current induced by write/erase cycling stress, resulting in data retention degradation when scaling down the tunneling oxide [2]. Furthermore, the FG-to-FG coupling effect will limit the space between the cells, which is especially serious for NAND flash memory. Recently, SONOS (polysilicon–oxide–nitride–oxide–silicon) memory devices are attracting great interest as a possible replacement for the traditional floating-gate flash EEPROM device, due to the low voltage operation [4], simple process integration [5], elimination of drain-induced turn-on [6] and improved cycling endurance [7]. In addition, a SONOS memory device with a split gate can be fast programmed with low power consumption [8–10]. The programmed window can be more

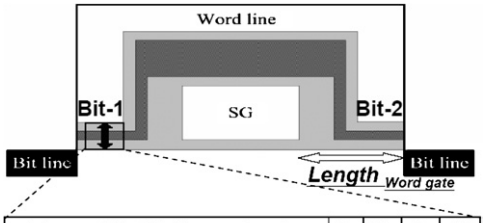
than 3 V in less than 1 μs. Furthermore, its novel wrapped-split-gate structure would also have faster programming speed [11] and more reliable performance [12] than the conventional SONOS cell. A fast and excellent control of the storage charge can be obtained even after large programming disturbance and $>10^4$ program/erase cycling. The superior charge retention behavior after high-temperature baking (>150 °C) of the WSG-SONOS memory is also presented for highly reliable multi-level and 2-bit/cell flash application.

In order to create high-density flash memory devices based on the same process technology [13–15], multi-level-cell (MLC) and/or 2-bit/cell operations are widely felt to be the most attractive approaches. Using MLC, the density of a flash memory device would be doubled, without any increase in the die size. Thus, a flash memory device with high density has been proposed as a mass storage requirement for portable terminals, solid-state cameras and PC cards [16–18]. Such an MLC would be constructed by storing different amounts of charge in the nitride trapping layers of a SONOS memory device. The different combinations of bits can be achieved by reliably distinguishing between the different levels in the SONOS memory device.

The concept of 2-bit/cell operation is a two-bit flash cell based on charge storage in an ONO dielectric [19–21]. One flash cell can store two physically separated bits by using a novel reverse reading scheme. The SONOS memory will thus have simpler processes and double density using the 2-bit storage. Nevertheless, critical issues for this 2-bit/cell application remain, including charge redistribution during programming [22], charge diffusion in silicon nitride after injection [23], and bottom oxide charge by cycling [21]. These limit MLC and 2-bit/cell application. A lateral migration phenomenon of the trapped charge after the charge injection will aggressively affect the multi-level differentiation. This makes it more difficult to obtain fully localized charge injection in the program and fully neutralize the electrons in the erase for both multi-level and 2-bit/cell operation.

Furthermore, multi-level operation cannot be easily achieved by conventional channel hot electron (CHE) injection [24–26] or Fowler–Nordheim (FN) tunneling [27], due to the resultant low efficiency of electron injection, poor programming speed and high operating voltage. Consequently, a novel operating mode called source-side injection (SSI) has been proposed and demonstrated for the split-gate SONOS memory structure, in order to attain high-speed programming and high efficiency of electron injection [10, 28]. The SSI method can effectively decrease programming time and achieve multi-level operation more easily. However, the dependence of different ONO thicknesses on the WSG-SONOS memory with the SSI mechanism has yet to be investigated in detail. In addition, multi-level programming of the WSG-SONOS memory device through the SSI mechanism has not been well developed.

In this paper, for the first time, we demonstrate the source-side injection mechanism of the WSG-SONOS memory with differing ONO thicknesses while successfully achieving a highly reliable multi-level and 2-bit/cell operation. The optimized ONO thickness of the WSG-SONOS memory is also obtained. We found that this WSG-SONOS memory with optimized ONO thickness meets the requirements of both the LSTP (low stand-by power) limitation and high-performance application. Moreover, multi-level and 2-bit/cell operation can easily be achieved in this WSG-SONOS memory with low programming current. It provides a fast, excellent control of the stored charge even after large programming stress and 10^4 program/erase cycling. This highly reliable multi-level operation using source-side injection for the WSG-SONOS memory also presented good charge retention behavior after high-temperature baking.



Top oxide thickness (nm)	9	10	9	10
Trapping nitride thickness (nm)	8			
Bottom oxide thickness (nm)	5	5	6	6
Total ONO thickness (nm)	22	23	23	24

Figure 1. Cross-sectional scheme of a 2-bit/cell WSG-SONOS memory device with wrapped-select-gate (WSG) structure. The different ONO thicknesses are summarized in the inset table.

2. Experiments

Figure 1 depicts the cross-sectional structure of the WSG-SONOS device with a cell size of 3.5 F^2, using the 0.18 μm ground rule technology. The channel length of the word gate is 0.12 μm, which is defined by the distance between the select-gate and bit-line region, as shown in figure 1. This device with the select gate wrapped around both an oxide–nitride–oxide (ONO) layer and a word-line gate as an assist gate was fabricated in order to achieve the source-side injection. The following were the key fabrication steps in the creation of the WSG-SONOS memory. (1) Select-gate (poly-silicon) deposition and patterning. The *in situ* n^+-doped poly-Si with 150 nm was deposited by a vertical furnace at 550 °C. (2) Silicon nitride of 300 nm thickness was deposited by low pressure chemical vapor deposition (LPCVD) at 780 °C on the select gate in order to isolate the word gate and the select gate. (3) The tunneling oxide was thermally grown at 925 °C under conditions of O_2 atmosphere to a thickness of 5 or alternatively 6 nm. (4) The trapping nitride was also deposited by LPCVD to 8.0 nm thickness. (5) The blocking oxide (TEOS) was deposited by LPCVD to 9.0 and 10.0 nm thicknesses. (6) Word-gate (poly-silicon) deposition (the same as select-gate deposition). The different ONO thicknesses of the WSG-SONOS memory device are summarized in figure 1. Thus, in this work, we use a common nitride thickness and alter the bottom and top oxide thickness in order to study their effect in the operation and reliability characteristics of the WSG-SONOS memory device. This simple fabrication procedure is

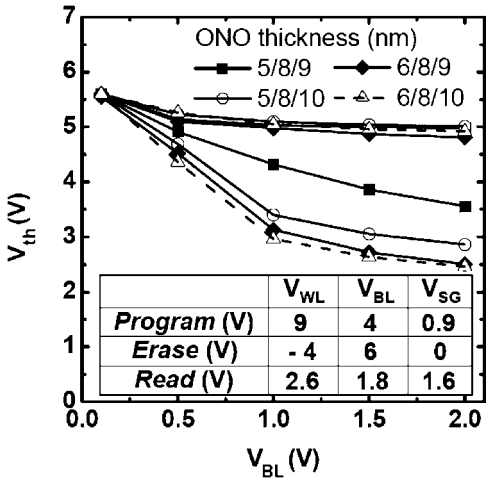


Figure 2. Excellent 2-bit/cell characteristics obtained for the WSG-SONOS memory with increasing ONO thickness. The basic operating conditions of the WSG-SONOS memory are listed in the inset table.

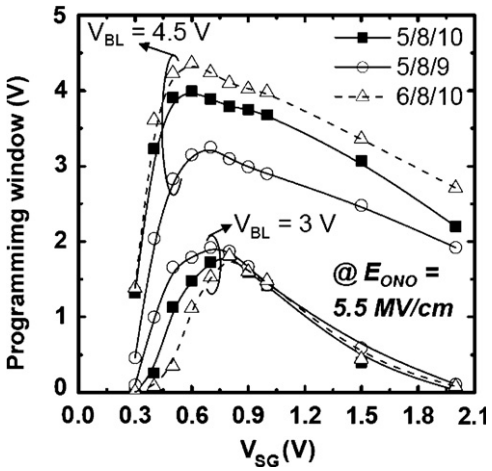


Figure 3. Programming characteristics of the WSG-SONOS memory for various ONO thicknesses under different applied select-gate biases.

easily compatible with conventional processes for fabrication of the CMOS-integrated circuit.

3. Results and discussion

3.1. Two-bit/cell operation of the WSG-SONOS memory

The source and drain regions were defined as the bit line in the WSG-SONOS memory to achieve the 2-bit/cell operation. Reading is performed in the 'reverse' direction, a 'reverse-read' scheme [29], by raising the right bit-line (bit-1 region) voltage and keeping the left bit-line (bit-2 region) grounded. The basic two-bit operating conditions of the WSG-SONOS memory in this paper are listed in the inset table of figure 2. The WSG-SONOS memory is programmed by performing source side injection as mentioned above. The characteristics of two-bit operation for the WSG-SONOS memory device with four different ONO thicknesses are shown in figure 2. This 2-bit/cell operation (only bit-1 was programmed, while bit-2 was in the initial state) of WSG-SONOS memory can be easily achieved for all samples as shown in figure 2. Figure 2 also shows that the clear two physical bits storage characteristic of our WSG-SONOS memory is demonstrated from the threshold voltage difference of these two bits, which can reach up to 1.5–2.5 V during reading while the drain and source were biased at 1.8 V and 0 V, respectively. Furthermore, the threshold voltage difference increases with the increasing ONO thickness of WSG-SONOS memory (figure 2). This phenomenon means that a thicker ONO layer will improve the 2-bit/cell characteristics. The length of the channel word gate is controlled by the ONO thickness. Thus, a longer length can aggressively separate the bit-1 and bit-2 regions to improve the two bit storage characteristics. In general, the tunneling oxide grown on the side wall of the doped poly-silicon (select gate) was thicker than on single-crystal Si. That explains why the threshold voltage difference increases from 2 to 2.3 V for WSG-SONOS memory with thin tunneling oxide (5/8/10), than with greater tunneling oxide thickness (6/8/9). The WSG-SONOW memory with thicker tunneling oxide will exhibit better 2-bit/cell characteristics while devices have the same ONO thickness. To sum up, the thicker tunneling oxide and ONO thicknesses, the better 2-bit/cell characteristics can be observed for WSG-SONOE memory.

3.2. SSI mechanism for the WSG-SONOS memory with different ONO thickness

Figure 3 shows the programming characteristics of the WSG-SONOS memory for different ONO thicknesses under different select-gate biases. The WSG-SONOS memory was programmed by applying the same ONO electric field (5.5 MV cm^{-1}) and different bit-line biases (3 and 4.5 V) at 10 μs. The results indicate that the select-gate bias (V_{SG}) dominates the programming efficiency, which is consistent with previous work [10, 11]. The reason for this phenomenon is that the variation in the lateral potential induces the change of lateral electric field in the SONOS device [30]. When the select-gate voltage (V_{SG}) is larger than the threshold voltage (V_{TH}), the potential beneath the select gate drops due to the effect of the bit-line voltage (V_{BL}) which decreases the lateral electric field, resulting in a small shift of the threshold voltage under electron injection. Similarly, when $V_{SG} < V_{TH}$, V_{BL} cannot induce a potential drop beneath the select gate, a larger threshold voltage shift results (figure 3). Furthermore, the programming efficiency is higher for thin ONO stacks (5/8/9) at low V_{BL} ($V_{BL} = 3$ V); while at high V_{BL} ($V_{BL} = 4.5$ V), it is higher for thick ONO stacks (6/8/10). This is also revealed in figure 4 with respect to V_{BL} for the programming efficiency, in which crossover is found at $V_{BL} = 3.5$ V for the WSG-SONOS memory under ONO thicknesses.

This phenomenon may be explained by simulation results using the integrated systems engineering (ISE) TCAD simulation tool shown in figure 5. In addition, some physical parameters including mobility, recombination and effective intrinsic density should be fed into the simulation. Devices with thin ONO stacks (5/8/9) exhibited larger lateral electric field than devices with thicker ONO stacks (6/8/10) under

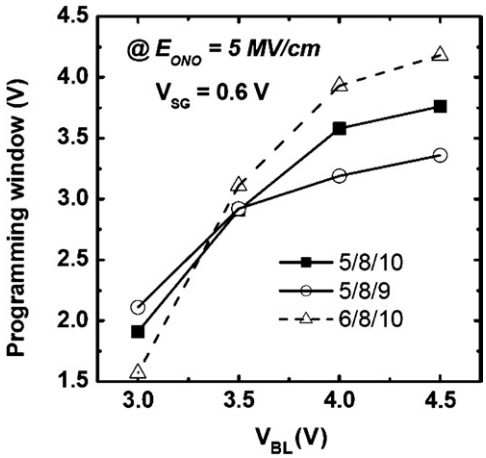


Figure 4. Programming characteristics of the WSG-SONOS memory with different ONO thicknesses under different applied bit-line biases.

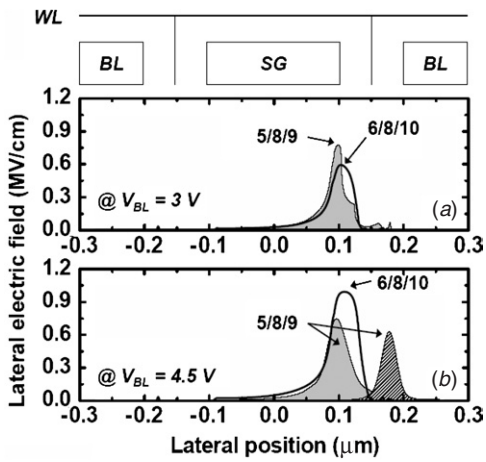


Figure 5. Simulation results show that the electrical field at the gap is saturated for thin ONO layers (5/8/9) when the bit-line bias is increased, but thicker layers (6/8/10) are not saturated.

small $V_{BL} = 3$ V (figure 5(*a*)). That is why the programming efficiency of devices with thin ONO layers was much higher than those with thick ONO. The larger lateral electric field results in the higher programming efficiency of WSG-SONOS memory. On the other hand, the larger V_{BL} did not affect the electric field at the gap for the thin ONO stacks (5/8/9) except for the increase in the electric field at the p–n junction; while for thick ONO stacks (6/8/10), the electric field at the gap increased gradually (figure 5(*b*)). The gap region is defined by the distance between the select-gate and trapping nitride (side-wall). The electric field at the gap of the thicker stack is clearly larger than at the gap of the thinner stack (figure 5(*b*)). This result explains why the programming efficiency of the thicker one is higher than the thinner one when the device was programmed at a large V_{BL} (=4.5 V). In summary, this research shows that the 'trade-off' in ONO thickness (5/8/10) exhibited by the WSG-SONOS memory offers optimized programming performance, which can meet both the LSTP (low operation voltage) limitation and high-performance (large programming window) applications.

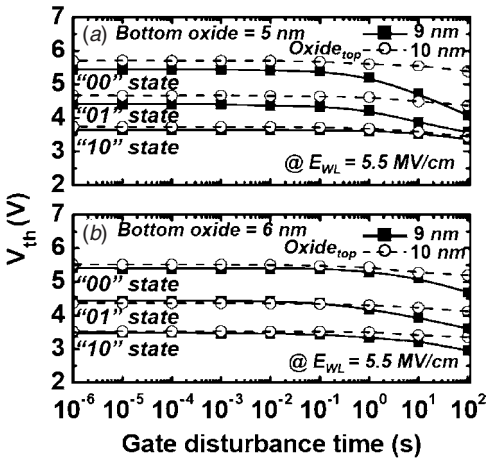


Figure 6. Gate disturbance performance of the WSG-SONOS memory with different ONO thicknesses for multi-level operation. The thick top oxide contributes to better gate disturbance.

3.3. ONO thickness optimization for the WSG-SONOS memory

The phenomenon of failure of the 'program inhibit characteristics', often takes place under electrical stress applied to neighboring un-programmed cells during programming of a specific cell in the array. Two types of program inhibit characteristics, gate (word line) disturbance and drain/source (bit-line) disturbance, need to be considered. In gate disturbance, a high electric field built across the tunnel oxide leads to unintentional tunneling of the electron out of the trapping nitride layer. Figure 6 demonstrates the gate disturbance performance of the WSG-SONOS memory with different ONO thicknesses for the multi-level operation. In order to achieve multi-level operation, the word-line biases had 9, 10 and 11 V applied to them to achieve the '10', '01' and '00' states (programming time is 1 μs), while the drain, source and select gate were biased at 4, 0 and 0.9 V, respectively. Figure 6 clearly shows that the thick top oxide will contribute to better gate disturbance when the bottom oxide thickness is different, in the WSG-SONOS memory device. Its deviation by the gate disturbance of the WSG-SONOS memory with a thick top oxide stack (10 nm) is found to be less than 0.2 V after 100 s of stresses for all states. However, serious gate disturbance characteristics were observed in devices with thin top oxide stacks (9 nm) (figure 6). The margins between neighboring V_t levels of multi-level operation were totally confounded after 100 s of stresses, especially for devices with the thinnest ONO layers (5/8/9). On the other hand, band-to-band-tunneling [29] is the main cause of drain disturbance, resulting in charge injection into the trapping nitride layer. However, the drain disturbance is not affected by the different ONO thicknesses in the WSG-SONOS memory (figure 7). The V_t shift of the drain disturbance was almost the same for devices with different ONO thicknesses after 100 s of stresses. Only a small negative shift in the '00' state was observed, due to the drain field inducing hole injection by band-to-band-tunneling [29]. As a result, the drain disturbance can be nearly ignored for other multi-level states for the WSG-SONOS memory.

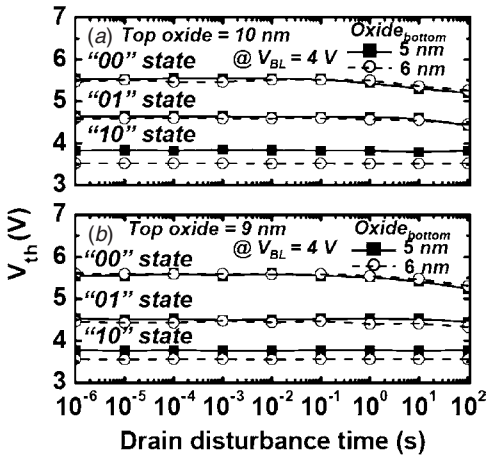


Figure 7. Drain disturbance performance for multi-level operation was not affected by the WSG-SONOS memory with different ONO thicknesses.

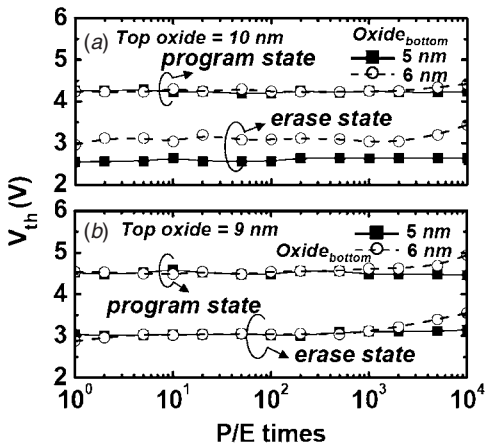


Figure 8. The endurance characteristics of the WSG-SONOS memory with different ONO thicknesses. Better endurance for the thin bottom oxide (5 nm) owing to the less interface states generation is shown.

Figure 8 shows the endurance characteristics of the WSG-SONOS memory with different ONO thicknesses. Here, the programming was done by the source-side injection while the erase was done by conventional band-to-band hot hole erasing. The measured condition of the multi-level operation is programmed with $V_{WL} = 9$ V, and $V_{BL} = 4$ V for 10 μs, and erased with $V_{WL} = -4$ V and $V_{BL} = 6$ V for 5 ms. For the device with thick tunneling oxide (6 nm), however, the window is preserved but both values increase with repeated cycling, indicating incomplete erasure [31] or more interface state generation in the tunneling oxide. The thin bottom oxide exhibits better P/E cycling performance, resulting in the negligible V_{TH} shift owing to the lower interface state generation (figure 8). In addition, the different top oxide thicknesses do not affect the cycling performance of the WSG-SONOS memory. In summary, the optimized ONO thickness (5/8/10) used in the WSG-SONOS memory has been demonstrated to achieve high performance and superior reliability.

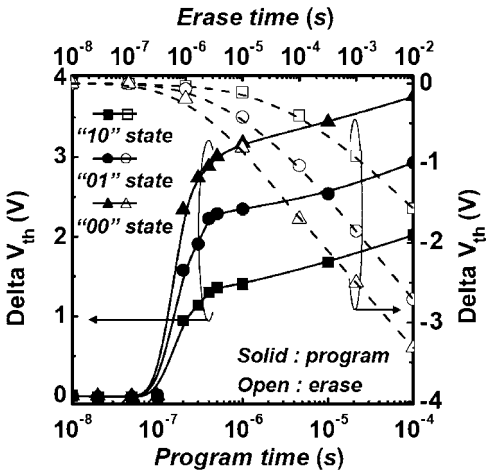


Figure 9. The programming and erasing characteristics of the WSG-SONOS memory with multi-level operation. The V_{TH} shift is larger than 1, 2 and 3 V at $V_{SG} = 0.9$ V, while the programming time is only 1 μs for $V_{WL} = 9$, 10 and 11 V, respectively.

3.4. High-performance multi-level operation for the WSG-SONOS memory

The WSG-SONOS memory with optimized ONO thickness (5/8/10 nm) was programmed by the source-side injection mechanism. In order to achieve multi-level operation, 9, 10 and 11 V were applied to the word gate while the drain, source and select gate were biased at 4, 0 and 0.9 V, respectively. Therefore, a word line biased at 9, 10 and 11 V to achieve the '10', '01' and '00' states (programming time (T_p) is 1 μs) can easily be obtained (figure 9). The device is reverse-read at $V_{WL} = 2.6$ V, $V_{BL} = 1.8$ V, $V_{SG} = 1.6$ V, respectively, as mentioned above. Similarly, with an erasing time of only 5 ms for $V_{WL} = -4$ V and $V_{BL} = 6$ V, multi-level operation can easily be accomplished. Moreover, the program level is not the same before erasing ($V_{WL} = 9$, 10 and 11 V, $V_{BL} = 4$ V), but the erasing voltages ($V_{WL} = -4$ V, $V_{BL} = 6$ V) are all the same for the different programming states in this work. Our results show that the erasing characteristics were easily controllable for the WSG-SONOS memory in multi-level application (figure 9).

The I_D–V_G transfer characteristics and excellent distribution of threshold voltage in different programming states were shown in figures 10(*a*) and 10(*b*), respectively. The word-line biases had 9, 10 and 11 V applied to them to achieve the '10', '01' and '00' states (programming time is 1 μs), while the device was reverse-read at $V_{BL} = 1.8$ V. We can see that tight V_t distribution and good margins were observed in this work, and the margins between the neighboring V_t levels ranged from 0.83 to 0.88 V. The window of state-to-state is larger than 0.8 V for programming at $V_{SG} = 0.9$ V and the T_p is only 1 μs. Furthermore, the high linearity between cell V_{TH} and V_{WL} for multi-level programming with different select-gate and bit-line bias is shown in figure 11. The linear dependence between the V_{TH} and the word-gate bias shows excellent performance with the different bit-line bias and select-gate bias for the WSG-SONOS memory with optimized ONO thickness. Furthermore, this high programming speed is

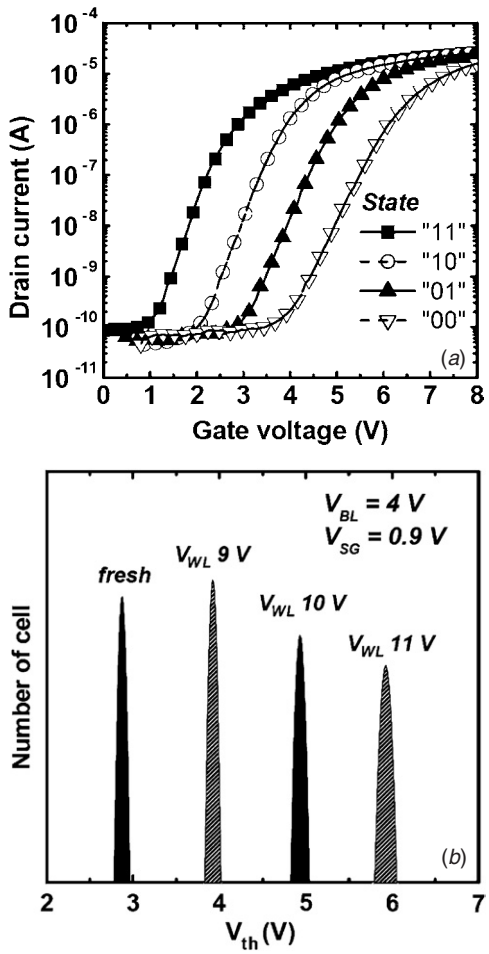


Figure 10. The (*a*) multi-level operation for experimental I_D–V_G characteristics, and (*b*) distribution of threshold voltage in different programming states, respectively.

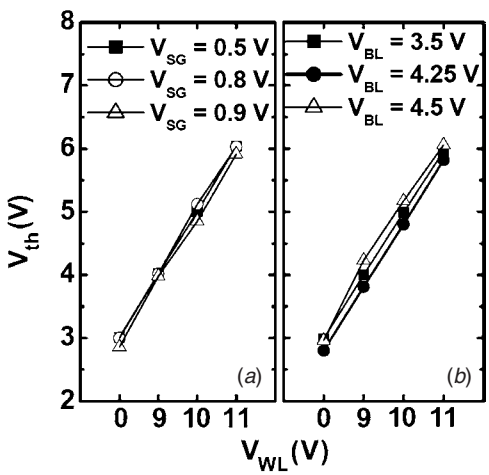


Figure 11. The linearity between V_{TH} and V_{WL} for multi-level programming operation in different (*a*) select-gate bias and (*b*) bit-line bias, respectively.

easily achieved by quite low programming current, less than 3.5 μA ('00' state) as indicated in figure 12. The programming currents of WSG-SONOS memory were 3.25, 3.00 and 2.75 μA for the '00', '01' and '10' states, respectively. The

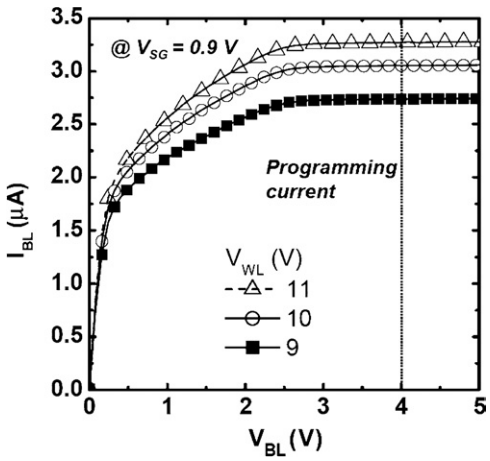


Figure 12. The bit-line current with different V_{WL} (9, 10 and 11 V). This result means that the programming current for different states was less than 3.5 μA.

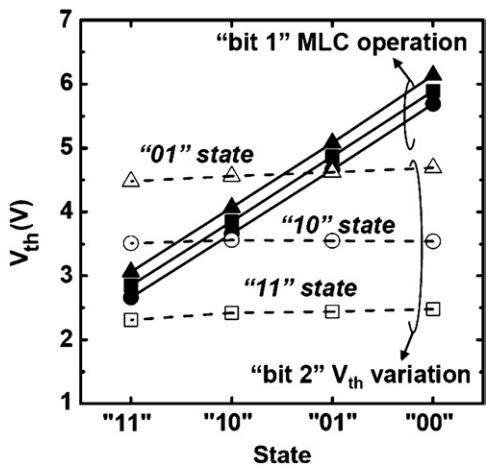


Figure 13. The excellent second bit effect characteristics of WSG-SONOS memory in different states with multi-level programming.

programming current will be only 1.4 mA for a 512-bit flash memory with multi-level operation, when the applied select-gate bias is 0.9 V. We believe that the high-speed programming performance of the multi-level operation should be attributed to the high injection efficiency of the source-side injection mechanism.

The cross-talk immunity between two cells sharing common control gate can be easily obtained for multi-level operation in the WSG-SONOS memory (figure 13). This figure demonstrates the second-bit effect characteristics at each state of multi-level operation. Fortunately, there is almost no second-bit effect induced degradation in this work, as figure 13 makes clear. In addition, the cross-talk between two cells sharing a common control gate may become significant for the WSG-SONOS memory as the device is scaled down. To avoid this, research should seek the optimized select-gate and bit-line bias to achieve the right state without the second-bit effect. Thus, a high performance and the scaled WSG-SONOS memory without cross-talk problem may become a reality.

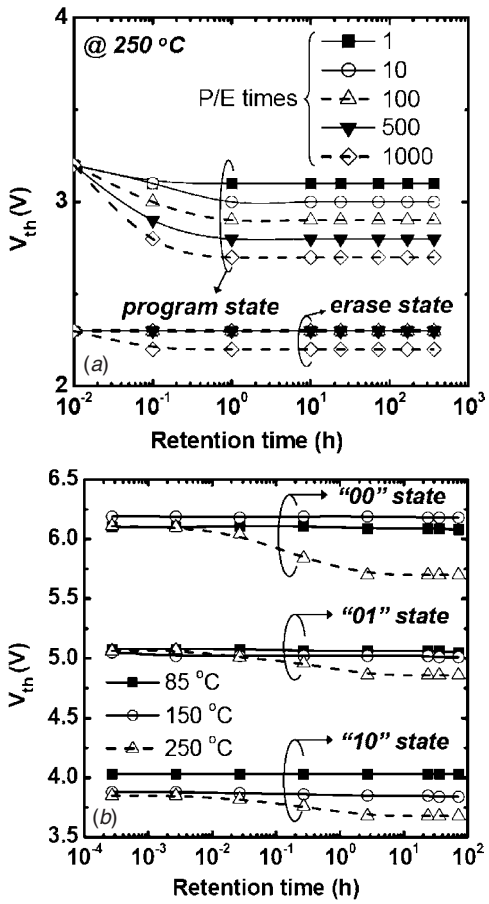


Figure 14. The data retention performance of the WSG-SONOS memory (*a*) with different P/E cycling times, and (*b*) at different high-temperature bakings with multi-level operation, respectively.

Figure 14 shows the data retention behavior of the WSG-SONOS memory (*a*) after different P/E cycling times, and (*b*) with multi-level operation at different high-temperature (85, 150 and 250 °C) bakings, respectively. The charge loss at 250 °C is degraded with increasing the P/E cycling times for the program state, but is not serious for the erase state (figure 14(*a*)). This charge loss results from the detrapping process in which the trapped electrons tend to migrate and redistribute in the silicon nitride under high-temperature operation [29]. Fortunately, the charge loss of the WSG-SONOS memory saturates [32], with the result that the memory window was still larger than 0.5 V after 1000 P/E cycling times. On the other hand, there is almost no charge loss for the multi-level operation of the WSG-SONOS memory at 85 and 150 °C as indicated in figure 14(*b*). Only a small charge loss is observed at quite high temperatures (250 °C) for the multi-level operation. However, this charge loss at such a high temperature will saturate and the different states of multi-level operation may still be easily differentiated (figure 14(*b*)). Nearly negligible window narrowing for multi-level operation is observed, implying that high performance and high reliability flash memory using our WSG-SONOS structure is feasible.

4. Conclusion

For the first time, a novel WSG-SONOS memory with highly reliable multi-level and 2-bit/cell is demonstrated. Multi-level storage is easily obtained with fast program/erase speed, due to the use of source-side injection in the WSG-SONOS memory. Furthermore, to obtain better and more reliable WSG-SONOS memory performance, the ONO thickness (5/8/10 nm) must be optimized. The programming mechanism of the WSG-SONOS memory under differing ONO thicknesses was also thoroughly investigated in this work. We also found that as far as the second-bit effect is concerned, program inhibit characteristics can be ignored for multi-level storage in this memory device. The superior data retention and endurance characteristics suggest that this WSG-SONOS memory with multi-level and 2-bit/cell operation has great promise for future high-density and high-performance flash applications.

Acknowledgments

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References

[1] Semiconductors Industry Association 2005 International Technology Roadmap for Semiconductors
[2] Naruke K, Taguchi S and Wada M 1988 *IEDM Tech. Dig.* pp 424–7
[3] Lue H T *et al* 2005 *IEDM Tech. Dig.* pp 547–50
[4] White M, Yang Y, Ansha P and French M L 1997 *IEEE Trans. Compon., Packag., Manuf. Technol.* **20** 190–5
[5] Chan T Y, Young K K and Hu C 1987 *IEEE Electron Device Lett.* **8** 93–5
[6] Cho M K and Kim D M 2000 *IEEE Electron Device Lett.* **21** 399–401
[7] She M, Takeuchi H and King T J 2003 *IEEE Electron Device Lett.* **24** 309–11
[8] Mih R *et al* 2000 *VLSI Tech. Symp.* pp 120–1
[9] Breuil L, Haspeslagh L, Blomme P, Wellekens D, Vos J D, Lorenzini M and Houdt J V 2005 *IEEE Trans. Electron Device* **52** 2250–57
[10] Chang K T, Chen W M, Swift C, Higman J M, Paulson W M and Chang K M 1998 *IEEE Electron Device Lett.* **19** 253–5
[11] Tomyie H, Terano T, Nomoto K and Kobayashi T 2002 *VLSI Tech. Symp.* pp 206–7
[12] Wu W C *et al* 2007 *IEEE Electron Device Lett.* **28** 214–6
[13] Shen S J, Yang C S, Wang Y S, Hsu C H, Chang D T, Rodjy N and Wang A 1997 *IEDM Tech. Dig.* pp 287–90
[14] Yamada R, Sekiguchi T, Okuyama Y, Yugami J and Kume H 2001 *VLSI Tech. Symp.* pp 115–6
[15] Shen S J, Yang C S, Wang Y S, Hsu C H, Chang D T, Rodjy N and Wang A 2006 *IEDM Tech. Dig.* pp 287–90
[16] Specht M *et al* 2004 *IEDM Tech. Dig.* pp 1083–5
[17] Chun S S, Yih C M, Liaw S T, Ho Z H, Wu S S, Lin C J, Kuo D S and Liang M S 1999 *VLSI Tech. Symp.* pp 19–20
[18] Tsai W J, Zous N K, Wang T, Joseph Ku Y H and Lu C Y 2006 *IEEE Trans. Electron Device* **53** 808–14
[19] Chang Y W, Lu T C, Pan S and Lu C Y 2004 *IEEE Electron Device Lett.* **25** 95–7

[20] Eitan B, Pavan P, Bloom I, Aloni E, Frommer A and Finzi D 2000 *IEEE Electron Device Lett*. **21** 543–5
[21] Tsai W J, Zous N K, Lie C J, Liu C C, Chen C H and Wang T 2001 *IEDM Tech. Dig*. pp 719–22
[22] Lee Y K, Kim T H, Lee S H, Lee J D and Park B G 2003 *IEEE Digest of Silicon Nanoelectronics Workshop* pp 92–3
[23] Lusky E, Shacham-Diamand Y, Bloom I and Eitan B 2002 *IEEE Electron Device Lett*. **23** 556–8
[24] Yeh C C *et al* 2003 *IEDM Tech. Dig*. pp 173–6
[25] Nair P R, Kumar B, Sharma R and Mahapatra S 2004 *IEDM Tech. Dig*. pp 403–6
[26] Nair P R, Kumar B, Sharma R and Mahapatra S 2006 *J. Appl. Phys*. **99** 044502
[27] Lee C H, Choi K I, Cho M K, Song Y H, Park K C and Kim K 1997 *IEDM Tech. Dig*. pp 613–6
[28] Kawamura T, Sasago Y, Kurata H, Otsuga K, Noda S, Kozakai K and Kobayashi T 2005 *VLSI Tech. Symp*. pp 206–7
[29] Hsieh C S, Kao P C, Chiu C S, Hon C H, Fan C C, Kung W C, Wang Z W and Jeng E S 2004 *IEEE Trans. Electron Device* **51** 1811–7
[30] Tomyie H, Terano T, Nomoto K and Kobayashi T 2005 *Japan. J. Appl. Phys*. **44** 4825–30
[31] Cho M K and Kim D M 2003 *IEEE Electron Device Lett*. **24** 260–2
[32] Choi B Y *et al* 2005 *VLSI Tech. Symp*. pp 118–9