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Cerium oxide nanocrystals for nonvolatile memory applications

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The characteristics of silicon-oxide-nitride-oxide-silicon-type memories embedded with cerium oxide nanocrystals were demonstrated. They were fabricated by depositing a thin CeO_2 film on the SiO_2 tunneling layer and subsequently rapid-thermal annealing process. The mean size and aerial density of the CeO_2 nanocrystals embedded in SiO_2 are estimated to be about 8–10 nm and $(3-7)\times10^{11}/cm^{-2}$ after a high-temperature annealing with different ambients on 900 °C. The program/erase behaviors and data retention characteristics were described to demonstrate its advantages for nonvolatile memory device applications. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2821367]

In recent years, cerium dioxide (CeO_2), which has been extensively researched on as the buffer layer for $YBa_2Cu_3O_{(7-x)}$ (YBCO) on sapphire,[1] an electrolyte material of solid oxide fuel cells,[2,3] buried insulator for silicon-on-insulator,[4] and $PbZrTiCeO_3$ ceramics,[5] is used for gate dielectric materials lately,[6] etc. Many superior properties such as lattice nearly matched to silicon (a=0.5411 nm) and sufficiently high dielectric constant (~26) (Refs. 7 and 8) for cerium dioxide led to the high thermal stability on silicon and high scaling capacity. Silicon and metal nanocrystals (NCs) are widely studied as potential solutions to overcome the scaling limitations of the conventional flash memories for future nonvolatile, high density, and low power memory devices.[9–13] Recently, high-κ dielectric NCs on the SiO_2 tunneling layer for silicon-oxide-nitride-oxide-silicon (SONOS)-type memories have been proposed. Lin *et al.*[14] have reported a method of cosputtering Hf and Si in oxygen followed with high-temperature annealing to form the high-κ NCs for SONOS-type memory devices. However, the HfO_2 nanocrystal memory exhibits saturation windows in channel-hot-electron (CHE) program mode. You *et al.*[15,16] have proposed the sol-gel spin-coating method to form the high-κ NCs. This method may increase thickness of tunnel oxide and results in high operation voltage.

In this study, the CeO_2 NCs were produced by a thermal annealing in different ambients. SONOS-type memories were fabricated and the electrical properties were investigated. The CeO_2 NC memory devices have shown good electrical properties in terms of large memory window (>2 V) at P/E speed of 10/10 μs and a retention time up to 10^4 s with only 10% charge loss. Our results suggest that the CeO_2 NC formation technique is simple and reliable, which shows a good potential for the application of the future fast nonvolatile memories.[17–19]

P-type Si (100) substrates with a resistivity of 5–10 Ω cm were used. A thin CeO_2 layer was deposited on SiO_2 tunneling layer by an electron-beam evaporator at 10^{-6} Torr. The samples subsequently underwent rapid-thermal annealing (RTA) at 900 °C for 1 min in either O_2 or N_2 ambient to form self-assemble CeO_2 NCs. Afterward, all samples were deposited with a 24-nm-thick blocking oxide layer by using a low-pressure tetraethoxysilane system at 700 °C. A 200-nm-thick polycrystalline silicon (poly-Si) gate was deposited and patterned. The poly-Si gate and source/drain regions were implanted with arsenic ($5\times10^{15}/cm^2$, 20 keV), and the subsequent dopant activation annealing was performed at 950 °C for 15 s. Finally, the CeO_2 NC memory devices were completed after the substrate contact patterning and metallization. The electrical properties of such devices were measured using HP 4156B semiconductor parameter analyzer and HP 41501A pulse generator.

The cross-sectional transmission electron microscopy (TEM) images of the CeO_2 NCs embedded in the SiO_2 dielectric matrix for rapid-thermal N_2 (RTN_2) and O_2 (RTO_2) samples are shown in Figs. 1(a) and 1(b), respectively. No obvious difference in microstructure in terms of NC size and disturbution are formed between annealed samples. They showed a NC density of $(3-7)\times10^{11}/cm^2$. The average NC size was 8–10 nm. Crystallized NCs with obviously visible lattice fringes were evident in the insets. Figure 2 shows the ideal energy band diagrams of the CeO_2 NC memory devices. The charges may be trapped in electron and hole traps in the CeO_2 NCs or by charge confinement in the quantum

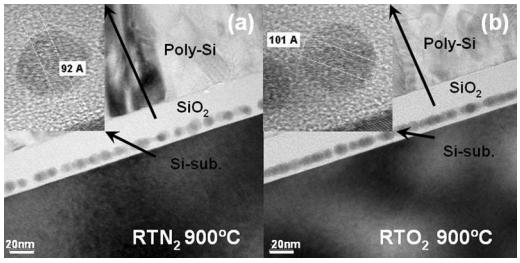

FIG. 1. Cross-sectional TEM images of the CeO_2 nanocrystals embedded in SiO_2 dielectric matrix: (a) with RTN_2 annealing at 900 °C for 1 min; (b) with RTO_2 annealing at 900 °C for 1 min, where the average nanocrystal size was 8–10 nm and obviously visible lattice fringes indicated crystallization of nanocrystals.

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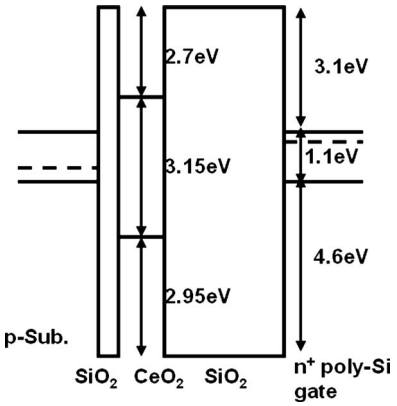
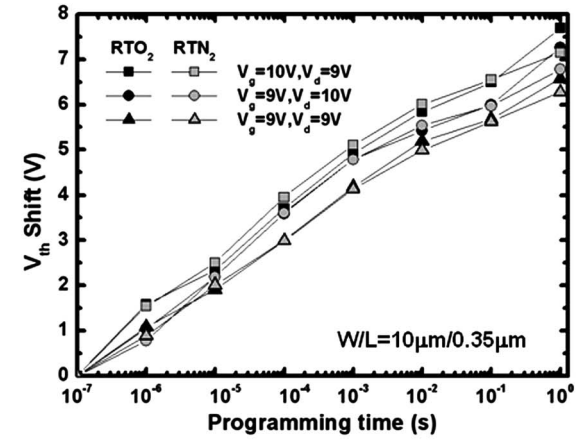


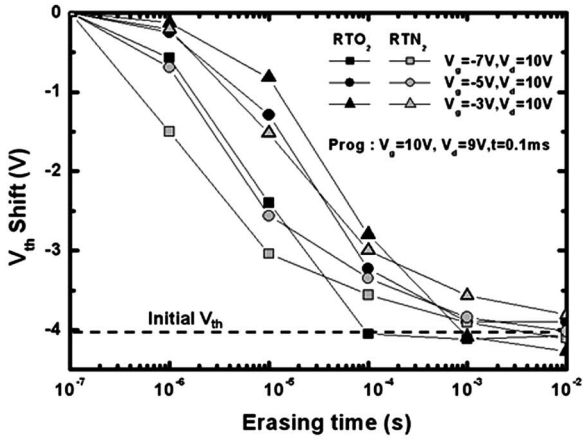
FIG. 2. Ideal energy band diagram for CeO_2 nanocrystal SONOS-type structures.

well.[17] Zhang *et al.*[20] have reported that the CeO_2 band gap is 3.15 eV and Engström *et al.*[21] have indicated that the conduction band offset between cerium oxide and silicon is 2.7 eV. The quantum well formed by the conduction band is deeper for CeO_2 NC structure than SONOS structure (2.7 eV compared to 1.05 eV).[22]

The programming speed of the CeO_2 NCs memory devices with RTN_2 and RTO_2 annealing are shown in Fig. 3(a).



(a)



(b)

FIG. 3. (a) Programming speed characteristics of CeO_2 nanocrystal flash memory devices with different programming conditions as a function of time. (b) The erasing speed characteristics of the CeO_2 nanocrystal memory cell at different erasing voltages.

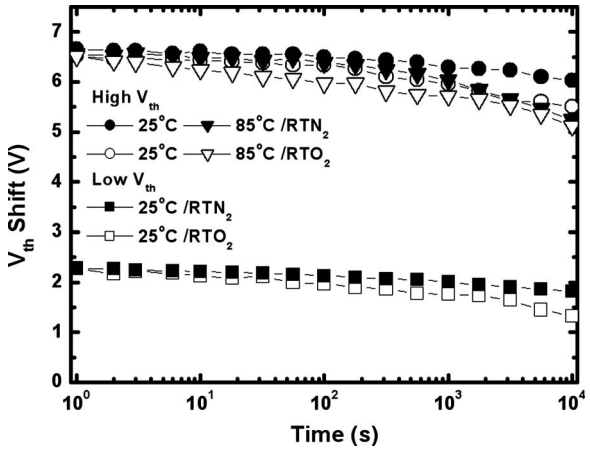


FIG. 4. Retention characteristics of CeO_2 nanocrystal flash memory devices with different RTA treatments and programming states.

The device is programed by CHE injection. When the program voltage increases to 10 V, the V_{th} shift increases rapidly and a memory window greater than 5 V was achieved within 1 ms. The large memory windows make the multilevel operation possible. The fact the programming speed is independent of annealing condition of the charge trapping centers, indicating that the programming speed is primarily dependent on the tunneling oxide. Figure 3(b) shows the erasing speeds at different voltages with a fixed V_d of 10 V. The device is erased band-to-band hot-hole (BBHH) injection. For the erasing speed operation, the device was programed under V_g=10 V, V_d=9 V with a duration of 0.1 ms. As observed, an increase in the negative gate bias resulted in a high erasing speed due to a higher electrical field for the BBHH injection. A fully erased state was fulfilled within 1 ms when operating two samples at V_g=−7 V and V_d=10 V. We concluded that using the CHE for programming and the BBHH for erasing has achieved high P/E efficiency in the CeO_2 NC memory devices.

Figure 4 shows the data retention characteristics of the CeO_2 NC memory devices with different RTA treatments and programming states. The RTN_2 sample showed a smaller amount of charge loss at room temperature for a retention times up to 10^4 s than the RTO_2 sample. It is conjectured that the bulk traps of RTN_2 sample are deeper than RTO_2 sample so that the charge loss of RTN_2 sample is less than RTO_2 sample. This phenomenon can be ascribed to the fact that sufficiently deep trap energy levels exist in the CeO_2 NCs. At high temperature (85 °C), RTN_2 sample increased charge loss rapidly after 10^3 s. The result is because the charge loss of RTN_2 sample comes from the charge in the bulk traps. The electrons can be either trapped in these bulk defects or stay in the conduction band of the CeO_2 NCs and/or in the interface states between the CeO_2 NCs and SiO_2.[17,22]

We have demonstrated higher P/E speed of 10/10 μs with CeO_2 NC memory devices. The RTN CeO_2 NC trapping layers have a larger charge storage capacity and a longer retention time up to 10^4 s with only 10% charge loss than the RTO sample due to deeper trap center. It is concluded that CeO_2 NCs can be used as discrete charge trapping sites for the SONOS-type memories.

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