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A flexible mixed-signal/RF CMOS technology for implantable electronics applications

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Abstract

A novel post-CMOS fabrication process has been developed to transform a 0.18 μm 1P6M mixed-signal/RF CMOS (complementary metal oxide semiconductor)-integrated circuit chips fabricated on an 8 inch SOI (silicon-on-insulator) wafer into flexible devices sandwiched between biocompatible material (10 μm parylene-C on both sides in this case) and enables future implementation of implantable and fully integrated electronic devices. The functionality of the flexible integrated circuits is demonstrated by a low phase noise RF CMOS VCO (voltage-controlled oscillator) circuit in a ring oscillator configuration that operates at a few hundred MHz to GHz. We report here the associated post-processing technology to make these flexible IC chips and the characterization of both MOS transistors and the demonstration circuit on the flexible IC chip under bending stresses.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Implantable electronic devices have drawn increasing attention for their applications in clinical diagnosis/monitoring and medical care [1]. The better these small, biocompatible, integrated-circuit devices are integrated with various micro sensing devices, the more medical applications they can be applied to (e.g. implantable sensors for monitoring blood pressure and flow and RF ID+ tags, artificial retina, etc). The additional characteristics of flexibility of these integrated devices are frequently desirable for many medical applications such as conforming to a curved surface, squeezing inside a stent, a small catheter tube or attaching them to soft tissues. However, most previous research on flexible thin-film electronic devices focused on the media applications. These include electronic paper, portable displays, etc based on organic thin film transistors technology. Although promising in the future, currently transistors based on these organic flexible materials typically show low mobility (from $\mu \sim 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) [2] and low integration densities and thus limited signal processing capability. Recent developments

in the backside illuminated CMOS image sensor have a thinned silicon substrate which will make the device more flexible; however, the silicon thickness (presumably several times of the few micrometers absorption lengths of visible lights in silicon) and the process details are not disclosed. For medical implant applications that require some local signal processing capabilities, we have developed a flexible post-CMOS technology based on a standard 0.18 μm 1P6M mixed-signal/RF CMOS process on 8 inch SOI wafers. This post-fabrication process removes the majority of silicon substrates of the integrated circuits and replaces them with flexible parylene-C (poly-para-xylylene C) films which are used as the substrate layer as well as the passivation layer for the circuits. Although not limited to this polymer, parylene-C is chemically inert, biocompatible and can be deposited by the chemical vapor deposition process at room temperature. These features make parylene-C a convenient material for post-processing. We developed the post-fabrication process utilizing parylene-C material to make flexible and potentially biocompatible integrated circuits, and use both the MOS transistor devices and a CMOS circuit (a voltage-controlled oscillator) to verify

the feasibility of this fabrication technology. The effects of stresses on these transistors are characterized for both compressive stresses and tensile stresses in longitudinal and transverse directions [3].

The ISO/DIS 10993 set entails a series of standards for evaluating the biocompatibility of a medical device prior to a clinical study. Parylene-C is an FDA approved Class-VI implantable plastic material with a long history of being used in pace maker and other implantable electronic packages [4–8]. It was tested as a chronically stable microelectrode insulator [4–6], proven successful in CNS (central nervous system) implants with minimal gliosis [5, 7], tested for its blood compatibility as an electronics-coating polymer film [8] and showed excellent result in cytotoxicity tests. This paper focuses on the technology and the characterization of parylene-based flexible transistors, but the study of biocompatibility is not covered and it should be assessed before clinical study.

2. Fabrication process

The flexible CMOS microsystem fabrication process used to implement the MOS transistor is outlined in figure 1. After the completion of a 1P6M 0.18 μm CMOS process on 8 inch SOI wafers with a 1 μm thick silicon epitaxial layer (figure 1(a)), the wafers are processed in a few more post-processing steps to make them flexible and potentially biocompatible as following. The post-CMOS process begins by depositing a 10 μm thick biocompatible parylene-C material to cover the circuit area (figure 1(b)). An adhesion promoter (silane A-174) is used to improve the adhesion of parylene to the silicon nitride passivation layer on the front circuit side. Parylene-C is selected due to its mechanical flexibility (Young's modulus ~ 3 GPa) and biocompatibility. The wafer is then bonded on the front side (already coated with the parylene-C layer) to a carrier substrate (figure 1(c)) in a wafer bonding machine. After bonding to the carrier substrate, the Si wafer substrate is mechanically thinned to a thickness of ~ 50 μm by a wafer lapping machine. The resulting surface micro-crack damages induced during the lapping process are removed by a silicon chemical etching (such as dry XeF_2 etching processes) with the buried oxide layer as the etch stop (figure 1(d)). Now the remaining silicon substrate is 1 μm thick. To protect the backside and balance the residual and in-use thermal stresses of the front-side parylene-C film, the backside substrate is coated by another parylene-C layer of the same 10 μm thickness (figure 1(e)). The adhesion promoter (silane A-174) is again used to improve the adhesion of parylene-C to the back substrate side. The remaining 1 μm thick silicon substrate in the region of dicing lanes is etched away before this second parylene deposition, so that the parylene-C layers on both sides of the wafer touch each other in this region and individual dies can be separated by a surgical knife.

To be able to characterize the transistors and circuits performance in a probe station, we open its electrical pads, although pads are not needed for passive circuit application. For this characterization purpose, the sandwiched structure is again bonded on the silicon substrate side to a carrier substrate (figure 1(f)), and the pads are opened (figure 1(g)) by oxygen

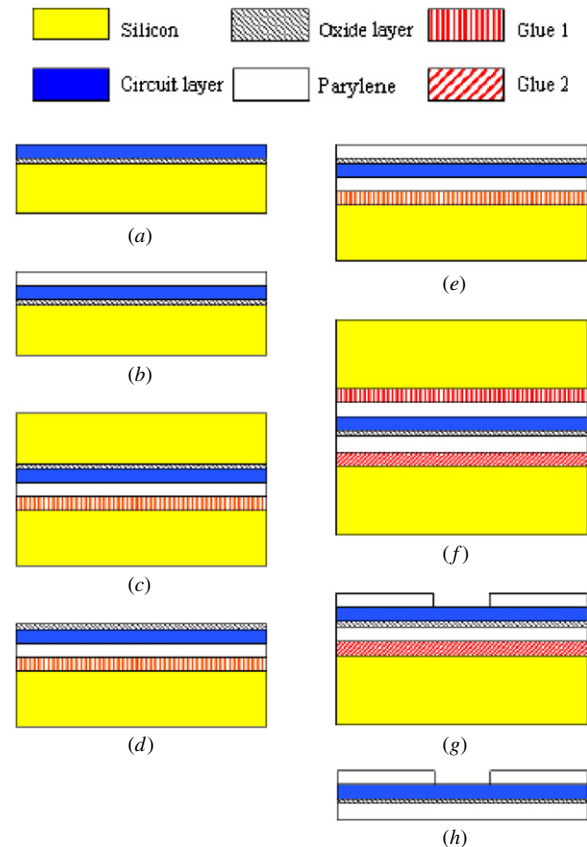


Figure 1. Fabrication process of a biocompatible flexible IC: (a) the SOI wafer with fabricated MOS transistors; (b) parylene coating on the front circuit side; (c) bonding the SOI wafer to a carrier substrate on the front side; (d) Si substrate is removed; (e) parylene deposited on the backside; (f) transfer of the wafer to another carrier substrate; (g) pad opening; (h) debonding SOI chip from the carrier substrate.

plasma RIE etch with the AZ 9260 photoresist as the masking material defining the pad opening area. The etching rate of parylene-C is $0.73 \mu\text{m min}^{-1}$ when the oxygen plasma was controlled at 200 W, 50 sccm and chamber pressure at 150 mtorr.

Finally, the flexible 8" wafers are de-bonded from carrier wafer (figure 1(h)) and can be cut into individual dies. The flexible CMOS wafers are sandwiched between and passivated by two parylene-C layers. The sandwiched structure consists of parylene-C film, silicon device layer ($\sim 1 \mu\text{m}$ thick) of the SOI wafer and parylene-C film. Since the remaining silicon device layer of the processed SOI wafer is only $\sim 1 \mu\text{m}$ thick, the circuit chip is semi-transparent even to light of shorter wavelength with photon energy more than the silicon band gap as shown in figure 2 with a piece of the flexible wafer placed in front of a color display (it also indicates that the flexible technology described in this paper will not be used in an optimized imaging sensor. An optimized imaging sensor needs thicker semiconducting layers of at least several photo absorption lengths in thickness to be efficient in photo-electron conversion.) Figure 3 shows the flexible CMOS wafer piece released from the carrier wafer after completing the post-process and cut into a stripe, and the slight curling of substrate piece was caused by both the residual stresses of



Figure 2. A semi-transparent flexible CMOS wafer piece (5 cm × 3 cm) after the process.

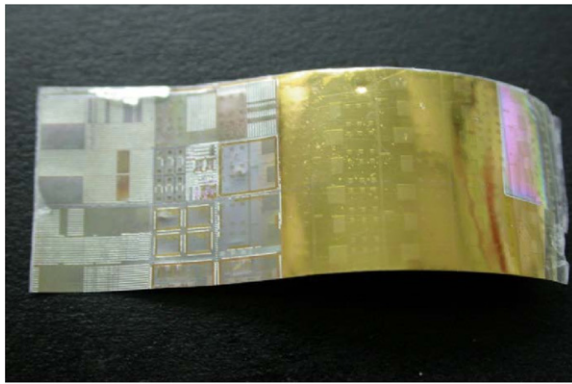


Figure 3. A biocompatible flexible CMOS wafer after the process (2 cm × 5 cm).

CMOS surface layers (oxide and metallization layers) and the stresses induced by the post-CMOS process. Since the maximum stress experienced by the chip under a bending to a fixed radius of curvature is proportional to the thickness of the chip, the very thin chip can be curled into a small radius of curvature. Repeating tests indicate that a stress level of ($\pm$) 100 MPa can be applied to devices safely. As shown in figure 4, a flexible CMOS wafer piece (~ 1.2 cm × 1.2 cm) can be curled into a cylindrical shape and inserted into a 4 mm ID (inner diameter) glass capillary tube to simulate the possible environment of potential applications such as inside a stent. The corresponding maximum stresses on the IC and devices in this case are around 180 MPa.

3. Characterization of the flexible transistors

The fabricated transistors have a channel length $L = 0.18$ μm , gate oxide thickness is 42 Å and channel width $W = 25$ μm . The test n-channel and p-channel field-effect transistors were fabricated on (1 0 0) silicon and the chips were made flexible by the above post-CMOS process. As shown in figures 5(a) and (b) for n-channel and p-channel transistors, the current to voltage characteristics were measured by a semiconductor parameter analyzer HP4156C in a probe station before and after the flexible post-processing, with the flexible transistor



Figure 4. A flexible CMOS wafer piece (~ 1.2 cm × 1.2 cm) curled into a cylindrical shape and inserted into a 4 mm diameter glass capillary tube.

Table 1. The measured threshold voltages of transistors before and after post-processing.

Transistor type	Threshold voltage (V)	
	Before process	After process
NMOS	0.567	0.560
PMOS	0.537	0.528

devices bonded to a carrier substrate in the latter case. The red lines are the characteristics of the MOS transistor measured before the post-processing, whereas the blue lines indicate the MOS transistor drain current to drain voltage curve measured after the post-processing. A slightly variation of the transistor drain current (less than 15%) after the post-processing steps was observed presumably due to enhanced bending from residual stresses of CMOS thin-film stack and interface defects created during the post-processing steps [11, 12]. The residue stresses of the metal (typically tensile) and oxide (typically compressive) stack of the CMOS deform the silicon substrate. This deformation will increase when the majority bulk of the silicon substrate is removed and this enhanced deformation induces further stresses on transistors and cause mobility change.

The threshold voltages of MOS transistors were obtained by measuring the I - V characteristics at a low drain to source voltage of $|V_{ds}| = 0.1$ V with a linear extrapolation method [10]. From the standard expression of the drain current of an n-channel MOSFET in the linear region [9],

$$I_d = (\mu_n C_{ox}) \left(\frac{W}{L} \right) \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right], \quad (1)$$

where μ_n represents the carrier mobility in the channel and C_{ox} is the oxide capacitance. V_t , V_{GS} and V_{DS} are the threshold voltage, voltage between gate to source and drain to source respectively. The transistor threshold voltages are derived from the x -intercepts of equation (1) at $V_t = V_{GS} - \frac{V_{DS}}{2}$, and the values before and after the post-processing steps for each type of MOSFETs are listed in table 1.

Since the implantable and flexible microsystems are intended to operate under external mechanical stresses, the effects of bending stresses on the MOS transistors are characterized. When a transistor is under mechanical stresses,

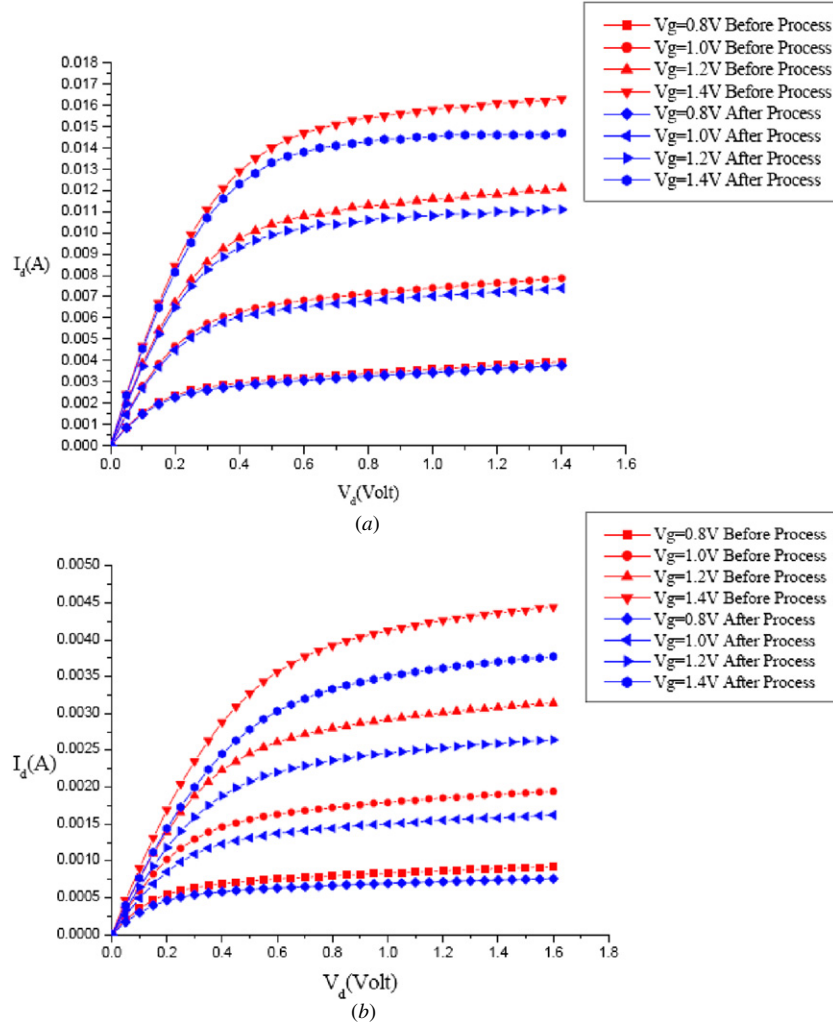


Figure 5. The measured transistor characteristics of drain current versus drain voltage before and after post-processing steps for (a) channel length $0.18 \mu\text{m}$ n-type MOS and (b) channel length $0.18 \mu\text{m}$ p-type MOS.

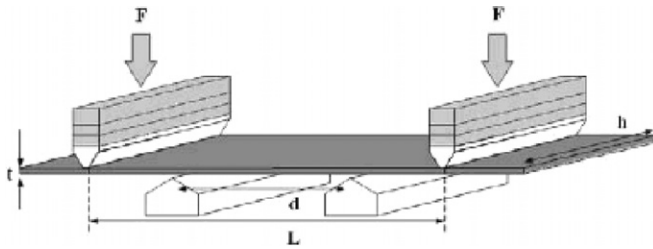


Figure 6. The schematics of the 4PB fixture used to generate uniform stress between the inner props.

the energy band structure will change, and thus the effective mass of carriers and the associate density of states, etc will vary accordingly. A four-point-bending (4PB) test setup as shown in the schematics of figure 6 is used to apply external mechanical stresses uniformly between the two inner points on the flexible chips and the actual 4PB fixture is shown in figure 7.

A uniform uniaxial stress between the middle two props is established on the surface and it can be shown to be

$$\sigma = \frac{3(L-d)F}{ht^2}, \quad (2)$$

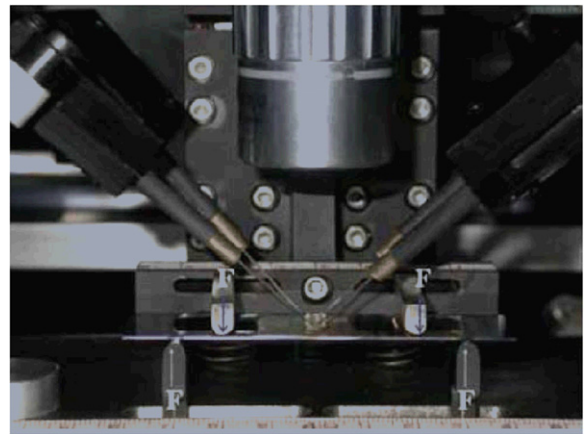


Figure 7. Actual 4PB fixture used in the experiment.

when the beam deformation is small and the dimensions of t and h are small in comparison to d and L , where t denotes the thickness of the plate, h the width of the plate, F the applied force, L the distance between the two upper

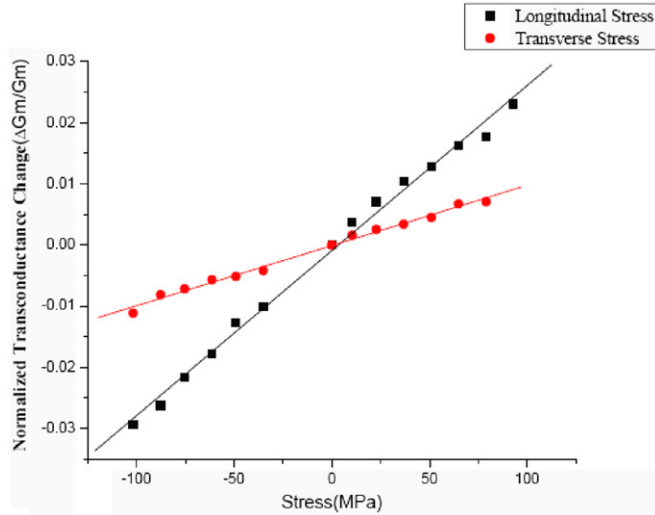


Figure 8. Normalized transconductance change versus applied stress of n-type MOS transistors under tensile and compressive stress in both the longitudinal direction and transverse direction relative to the transistors' channel direction.

props and d the distance between the two lower props. The applied stress can be either tensile or compressive depending on whether $d < L$ or $d > L$. The transconductance of the MOS transistors and the threshold voltages are extracted from its I - V characteristics when the channel and immediate surrounding region is under tensile or compressive stress (between -100 MPa and 100 MPa) in both longitudinal and transverse directions in reference to the channel length direction. Both n-type and p-type MOS transistors with channel length $L = 0.18 \mu\text{m}$ and the gate oxide thickness is $42 \text{ \AA}$ were used for stress characterization. A piece of the flexible IC containing these individual MOS transistors was bonded onto a rectangular silicon strip $500 \mu\text{m}$ in thickness. We kept the applied mechanical stress within $(\pm) 100$ MPa to avoid cracking the Si strip initiated from edge defects which occurred when the stress was approaching 200 MPa. The calibration of 4PB fixture was carried out by using a strain gauge (Vishay C061117-C) and Keithly 2410. The calibrated four-point bending jig is adapted to a shielded probe station to apply controlled uniform stresses (tensile or compressive) on the sample and the I - V characteristics are measured.

The drain current expression of n-channel MOSFET in the linear region is expressed as in equation (1) above, and we get the threshold voltage from the x -intercept of the I_d versus V_{GS} curves and the electron mobility from the slope $\text{Slope} = \mu_n C_{ox} (W/L) V_{DS}$.

The variation of threshold voltage and transconductance under stress can be measured from the slope and intercept of transfer characteristics of the transistor in the linear region as a function of applied stress. The measured percentage change of transconductance versus stresses relation is shown in figures 8 and 9. This normalized transconductance $\frac{\Delta G_m}{G_m}$ variation of the flexible MOS transistors under stresses can be fit by a linear relationship with the uniaxial stresses in both longitudinal and

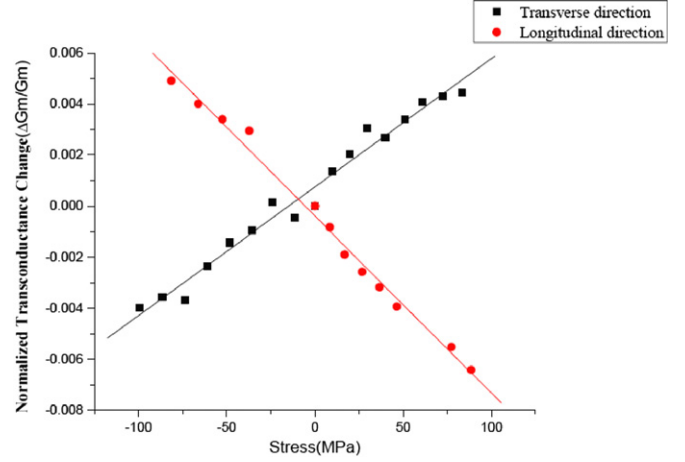


Figure 9. Normalized transconductance change versus applied stress of p-type MOS transistors under tensile and compressive stress in both the longitudinal direction and the transverse direction relative to the transistors' channel direction.

Table 2. Stress effects on a $0.18 \mu\text{m}$ MOS transistor.

Piezo parameters	NMOS devices ($\times 10^{-12} \text{ Pa}^{-1}$)	PMOS devices ($\times 10^{-12} \text{ Pa}^{-1}$)
Π_L	266	-69.4
Π_T	131	50.3

transverse directions as

$$\frac{\Delta G_m}{G_m} = \prod_{T(or L)} \sigma, \quad (3)$$

where Π_L is the longitudinal piezo-coefficient and Π_T is the transversal piezo-coefficient. It is also shown that $\sim(\pm) 3\%$ variation of transconductance change per 10^8 Pa stress in the longitudinal direction has been observed roughly twice of that in the transverse direction. However, the PMOS transistor changes only $(\pm) 1\%$ variation of transconductance. Table 2 summarizes the piezo-coefficients of the flexible transistors. The threshold voltage is found to only have small sensitivity to stress as shown in figure 10. These parameters will be used for pre-compensations in circuits design based on this technology.

4. Flexible circuit implementation and characterization

A low phase noise CMOS voltage-controlled oscillator in ring oscillator configuration is made on the flexible substrate as shown in the die photo figure 11 to assess the functionality of the flexible circuits after the post-processing. The oscillator circuit consists of four stages of differential pairs and each stage contains six p-MOS and three n-MOS transistors. The numbers of series connection stage alter the oscillation frequency caused by the delay of the oscillation signal. Figure 12 shows the schematic circuits of the tested ring oscillator. These four differential pairs in each stage consist of both p-MOS and n-MOS transistors as shown in

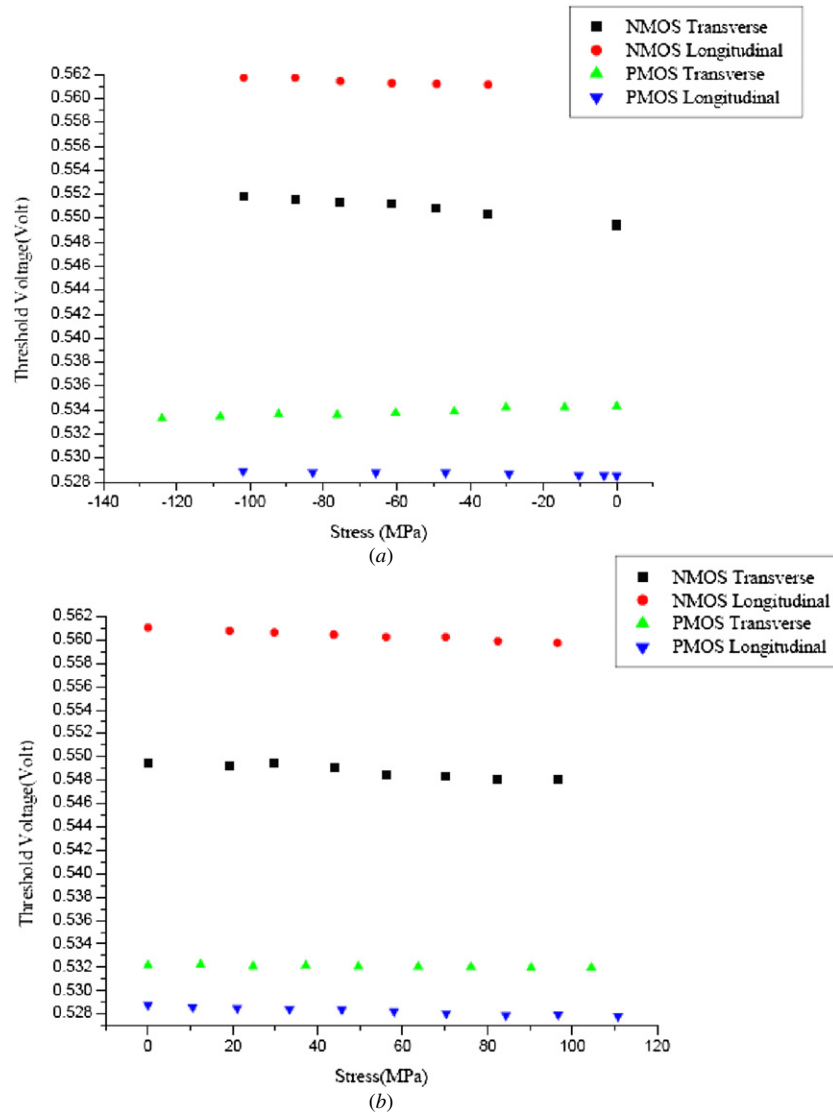


Figure 10. Measured MOS threshold voltage under (a) compressive and (b) tensile stress for both n- and p-type transistors in longitudinal and transverse directions.

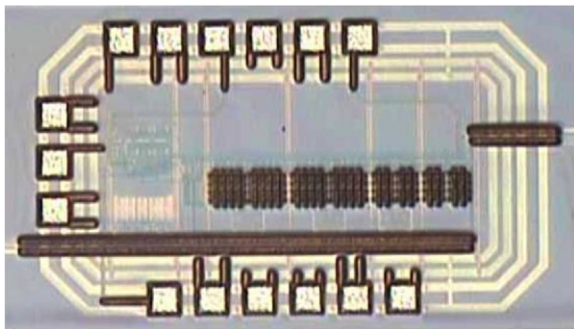


Figure 11. The die photo of the voltage-controlled oscillator made on the flexible substrate to assess the effect of post-CMOS processing described in the text ($1130\ \mu\text{m} \times 610\ \mu\text{m}$).

figure 13 with the sizes of the MOS transistors labeled. The differential pair circuit uses p-MOS transistors of the channel width of $W = 16\ \mu\text{m}$, $6\ \mu\text{m}$ and $3\ \mu\text{m}$, channel length $L = 0.5\ \mu\text{m}$, and n-MOS transistors with the channel length and

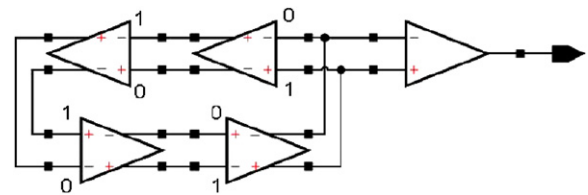


Figure 12. The schematic diagram of the ring oscillator configuration with 0/1 represents the input signal. Notice the cross-over of the wiring in the middle for this four-stage ring oscillator to make the oscillation.

width of $32\ \mu\text{m}$, $0.34\ \mu\text{m}$ and $2\ \mu\text{m}$, respectively. Figure 13 shows four differential pairs connection, where V_B is the bias voltage and V_C is the tuning voltage which controls the output resistance of p-MOS differential pair. Frequency is controlled by changing the V_B bias voltage and hence the delay through each n- and p-MOS transistors. The frequency spectrum was measured by a spectrum analyzer E4407B. The center

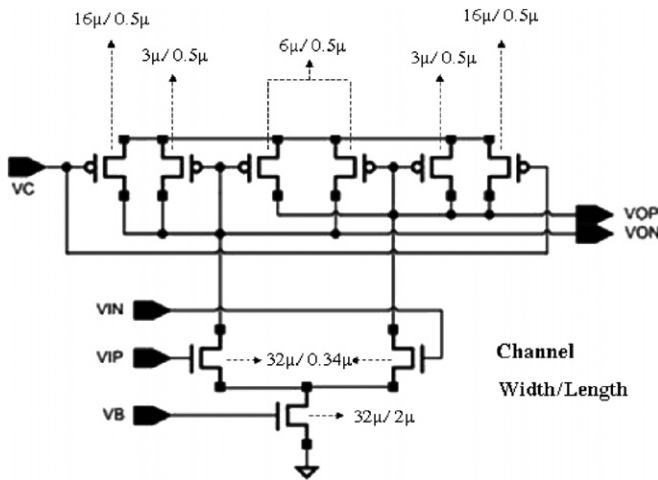


Figure 13. The circuit diagram of each differential pair stage in figure 12. The input VB is the bias voltage and VC is the tuning voltage which controls the output resistance of p-MOS differential pair.

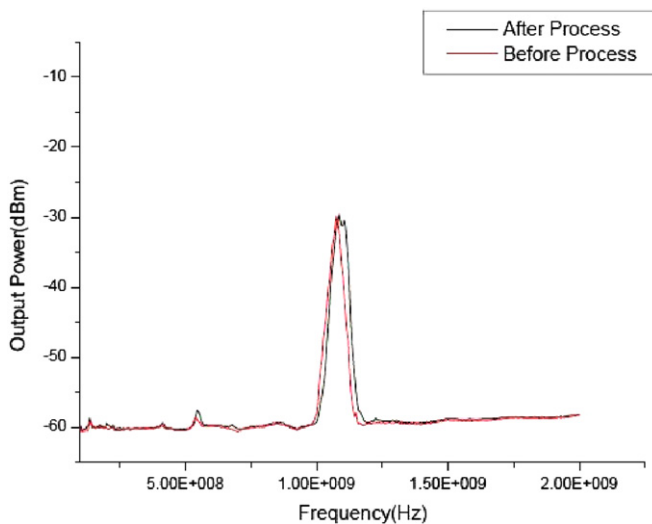


Figure 14. The measured VCO frequency spectrum has the center frequency at 1.08 GHz.

frequency of the oscillator is 1.085 GHz and power dissipation is 16 mW. The phase noise measured before and after this transform process is $-100.8 \text{ dBc Hz}^{-1}$ and $-98.83 \text{ dBc Hz}^{-1}$ respectively. Figure 14 shows the oscillation frequency before and after the post-processing. The oscillation frequency varies from 1.015 GHz to 750 MHz when the tuning voltage changes from 0.4 V to 0.9 V as shown in figure 15. Figure 16 shows the induced changes of oscillation frequency due to external stresses when the tuning voltage is fixed at 0 V. The oscillation frequency increases under compressive stress and decreases under tensile stress. Figure 17 shows the tuning of oscillation frequency under external stresses. This RF circuit was used with a simple division circuit for the frequency band of Medical Implant Communications Service (MICS) for 402–405 MHz, ISM band, which is an ultra-low power, unlicensed, mobile radio service band for transmitting data in support of diagnostic or therapeutic functions associated with implanted medical devices.

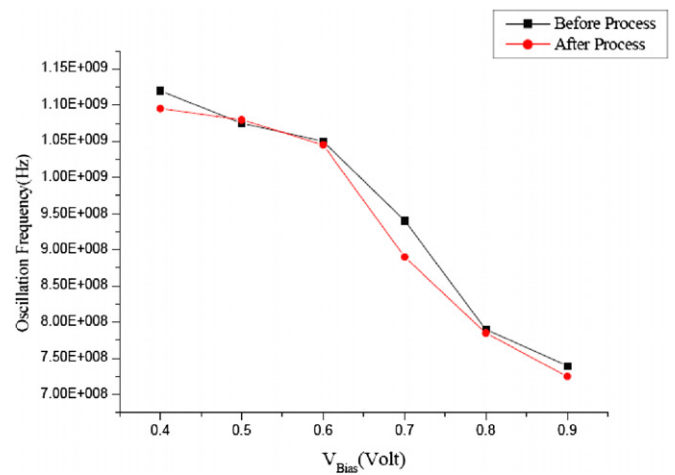


Figure 15. The measured characteristics of oscillation frequency versus tuning voltage before and after post-processing.

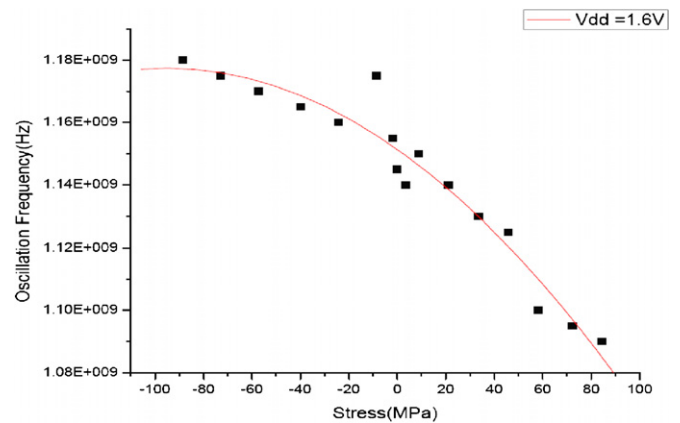


Figure 16. Measured oscillation frequency change under external stress.

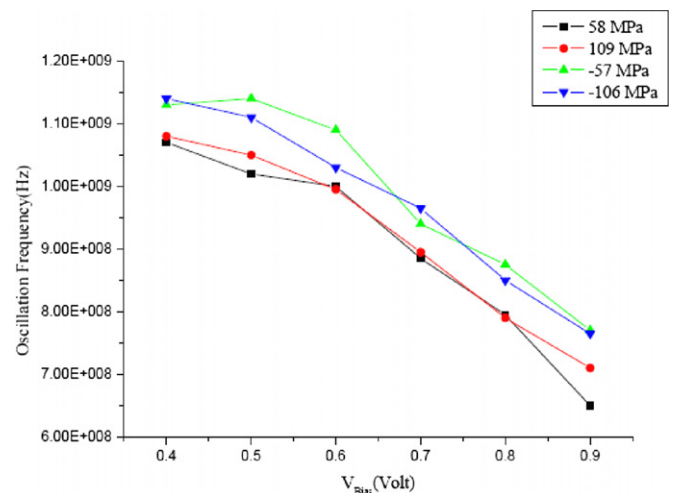


Figure 17. Measured oscillation frequency and bias voltage versus different stress conditions.

5. Summary and discussion

We have demonstrated a micro fabrication technology to make flexible $0.18 \mu\text{m}$ 1P6M mixed signal/RF CMOS

circuits for medical implant applications. Functionality of electronic devices and circuits are demonstrated with MOS transistors and GHz CMOS RF VCO made by this flexible technology. RF components can be implemented using this technology. Further implementation of CMOS-compatible MEMS components will allow the realization of compact and fully integrated implantable microsystems. Since these implantable devices will be used in some physical environments with applied external stresses and stress is known to change transistor characteristics [13–16], stress effects on these electronic devices and circuitry are characterized for pre-compensation in the circuit designs. Although the threshold voltages change very little for both nMOS and pMOS, the electron mobility in the n-channel device increases linearly with both longitudinal and transverse tensile stresses within the applied stress range reported here. The hole mobility in the p-channel device increases linearly with applied transverse stresses but decreases linearly with applied longitudinal tensile stresses. (When the applied stresses change sign to compressive, the effects also change reversely.) The transconductances of the nMOS and pMOS transistors in the ring oscillator change with the applied stresses, and this influences the charging and discharging time of the gates of the following stage and thus the resonant frequency. This can be applied to applications such as implantable RF stress sensors using these flexible CMOS circuits without additional transduction elements.

Acknowledgment

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