行政院國家科學委員會專題研究計畫 成果報告

奈米隨機存取記憶體的長時間可靠度劣化現象分析與可容忍此劣化現象之設計
研究成果報告(精簡版)

計 畫 類 別 ：個別型
計 畫 編 號 ：NSC 98-2221-E-009-112-
執 行 期 間 ：98 年 08 月 01 日至 99 年 07 月 31 日
執 行 單 位 ：國立交通大學電子工程學系及電子研究所

計畫主持人：莊景德
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報 告 附 件 ：出席國際會議研究心得報告及發表論文

公 開 資 訊 ：本計畫可公開查詢

中 華 民 國 99 年 10 月 31 日

附件一

行政院國家科學委員會補助專題研究計畫 ■成果報告 □期中進度報告

奈米隨機存取記憶體的長時間可靠度劣化現象分析與可容忍此劣化現象之設計

計畫類別：■個別型計畫　□整合型計畫

計畫編號：NSC　98-2221-E-9-112

執行期間：　98 年 8 月 1 日至 99 年 7 月 31 日

執行機構及系所：國立交通大學電子工程學系

計畫主持人：莊景德（教授）

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成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

本計畫除繳交成果報告外，另須繳交以下出國心得報告：

□赴國外出差或研習心得報告

□赴大陸地區出差或研習心得報告

■出席國際學術會議心得報告

□國際合作研究計畫國外研究報告

處理方式：除列管計畫及下列情形者外，得立即公開查詢

□涉及專利或其他智慧財產權，□一年□二年後可公開查詢

中　華　民　國　99　年 10　月 31　日

前言及文獻探討。

As CMOS technology is scaled down to deep sub-100 nm regime, leakage, variation, and long-term degradation have surfaced to constrain the scalability, attainable performance, and reliability. Long term degradation such as soft/hard oxide breakdown (BD) [1, 2] results in excessive gate leakage, while Host Carrier Effect (HCE), NBTI (Negative Bias Temperature Instability), and PBTI (Positive Bias Temperature Instability) [3-5] cause V_T drift over the life span of usage. In 6T SRAM cells, gate-to-source and gate-to-drain BD of pull-down NMOSs have been shown to significantly degrade the Read Static Noise Margin (RSNM) [2].

NBTI (Negative Bias Temperature Instability) has long been known as a limiting factor in the scaling of PMOS [3, 4]. At high negative bias and elevated temperature, the PMOS V_T gradually drifts to become more negative, thus reducing the PMOS current drive. The mechanism has been identified to be due to interaction of holes in inversion layer with Si-H bonds at interface, which leave interface traps (thus causing increase in $|V_T|$ under stress condition). When stress conditions are removed, H diffuses back to interface and passivates dangling Si-bonds. As a result, passivation (or partial "recovery" of V_T) occurs [3, 4, 5]. NBTI has been shown to degrade SRAM RSNM , while writability and leakage may improve with time [4]. Recently, with the introduction of high-k metal-gate technology, the Positive Bias Temperature Instability (PBTI) has emerged to be a major reliability concern for NMOS due to V_T instability caused by charge trapping at the interface [6]. PMOS NBTI and NMOS PBTI have been shown to lead to additive degradation in Vcc,min of 6T SRAM [7].

References

[1] Ben Kaczer, Robin Degraeve, An De Keersgieter, Koen Van de Mieroop, Veerle Simons, and Guido Groeseneken, "Consistent Model for Short-Channel nMOSFET After Hard Gate Oxide Breakdown," IEEE Trans. Electron Devices, vol. 49, no. 3, Mach 2002, pp. 507-513.

[2] R. Rodríguez, J. H. Stathis, B. P. Linder, S. Kowalczyk, C. T. Chuang, R. V. Joshi, G. Northrop, K. Bernstein, A. J. Bhavnagarwala, and S. Lombardo, "The Impact of Gate-Oxide Breakdown on SRAM Stability," IEEE Electron Device Letters, vol. 23, no. 9, Sept. 2002, pp. 559-561.

[3] G. Chen et al., "Dynamic NBTI of PMOS Transistors and Its Impact on Device Lifetime," Proc. International Reliability Physics Symp. (IRPS), 2003, pp. 196-202.

[4] Kunhyuk Kang, Haldun Kufluoglu, Kaushik Roy, and Muhammad Ashraful Alam, "Impact of Negative-Bias Temperature Instability in Nanoscale SRAM Array: Modeling and Analysis," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 10, Oct. 2007, pp. 1770-1781.

[5] http://www.eas.asu.edu/~ptm/.

[6] S. Zafar et al., "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO_2/HfO_2 Stacks with FUSI, TiN, Re Gates," Dig. Tech. Papers, Symp. VLSI Tech., 2006, pp. pp.23-25.

[7] J.C. Lin, A.S. Oates and C.H. Yu, "Time Dependent Vccmin Degradation of SRAM Fabricated with High-k Gate Dielectrics," Proc. International Reliability Physics Symp. (IRPS), 2007, pp. 439-444.

研究目的。

All these previous works, however, focused only on the standard SRAMs and cells. Many of the state-of-the-art low-power SRAM designs employ power-gating techniques to suppress leakages. As such, it is crucial to understand the impacts of gate-oxide BD and NBTI/PBTI degradation on the power-gating structure, in addition to the cell, and the resulting impacts on the power, performance, margin, and wake-up time, etc.. Further, performance-critical peripheral circuits such as PFET-type pre-charge circuit is also susceptible to NBTI, and high-performance differential sense amplifier can be particularly sensitive to the V_T mis-match/mis-tracking caused by NBTI and PBTI. Finally, most state-of-the-art SRAMs utilize replica-based Read/Write timing control scheme to mitigate the effects of excessive leakage and variation, and NBTI/PBTI induced V_T drifts can render the scheme ineffective or even useless.

研究方法。

In this project, using 32nm CMOS high-k Predictive Technology Model (PTM) calibrated with published hardware data, we carried out comprehensive analyses to include the impacts on various SRAM power-gating structures, sense amp, and peripheral circuits, to understand the resulting degradation in overall power, performance, and wake-up time, etc.. We also examined the timing control degradation caused by NBTI/PBTI on replica-based read/Write assist circuits. The analyses provided fundamental understanding and insights to facilitate the exploration and development of degradation-tolerant circuit schemes to enhance the reliability, lifetime, and scalability of nanoscale SRAMs.

We also collaborated with our former colleagues at IBM T. J. Watson Research Center to engage high-κ metal-gate Group for NBTI/PBTI model-to-hardware correlation/calibration, and SRAM and Technology-Circuit Co-Design members in VLSI Design Department to assess impacts of NBTI/PBTI on dynamic noise margin, cell failure probability, relative sensitivities and development of optimization guidelines based on performance or density requirements for application-specific target stability/performance.

結果與討論。

1. We carried out a comprehensive analysis on the impacts of NBTI/PBTI on power-gated SRAM arrays with high-k metal-gate devices and the combined effects with the contact resistance on SRAM cell stability, margin, and performance. NBTI/PBTI tolerant sense amplifier structures were also discussed.
   The results have been presented at ***2009 IEEE International Workshop on Memory Technology, Design, and Testing (MTDT), August 31-Sept. 2, 2009, Hsinchu, Taiwan.*** The full-length journal paper has been accepted by ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems.***

2. We provided comprehensive analyses on the impacts of NBTI/PBTI on a two-port 8T SRAM design, including the stability, Write Margin, Read/Write access paths, and Replica timing control circuits. We showed, for the first time, that because the Read/Write Replica timing control circuits were activated in every Read/Write cycle, they exhibited distinctively different degradation behavior from the normal array

access paths, resulting in degradation of timing control and performance. We also discussed degradation tolerant design techniques to mitigate the performance and reliability degradation induced by NBTI/PBTI. The full-length journal paper has been submitted to ***IEEE Transactions on Circuits and Systems***, and is under revision now.

3. We carried out a detailed analysis on the impacts of various gate-oxide breakdown (BD) paths in power-gated SRAMs. The gate-oxide breakdowns (BD) of the power-switches were shown to have severe and even detrimental effects on the margin, stability, and performance of power-gated SRAM. We also proposed and evaluated several techniques to mitigate the power-switch gate-oxide BD, including adding a gate series resistance to the power switch, dual threshold voltage power switch, thick gate-oxide power switch, and dual gate-oxide thickness power switch. It is shown that dual gate-oxide thickness power switch improves the time-to-dielectric-breakdown of the power switch while maintaining the performance without side effect. The results have been presented at ***2010 International Conference on IC Design and Technology (ICICDT), Minatec in Grenoble, France, June 2-4, 2010.*** The full-length journal paper has been accepted by ***Microelectronics Journal.***

4. Together with IBM, we analyzed the relative impacts of NBTI/PBTI on SRAM stability and access time. Monte-Carlo simulations were performed in a 45 nm PD/SOI technology to estimate the increase in cell failure probability with time, and design guide-lines for different application specific (high-performance versus low-power) SRAM cells were provided. The results have been presented at The results have been presented at ***2009 IEEE International Reliability Physics Symposium (IRPS). Montreal, Quebec, Canada.*** The full-length journal paper has been published in ***Journal of Microelectronics Reliability.***

5. We have filed **2** patents (a) Circuit techniques to mitigate the NBTI/PBTI effects in SRAM Write-Replica timing control circuit, and (b) Use of dual-oxide header/footer in SRAM power-gating structures to mitigate the power-switch gate-oxide breakdown effects.

   (a) Patent : “降低 NBTI/PBTI 效應於先進製程 SRAM 的寫入控制電路”,中華民國專利申請案號：098125793。美國專利申請中。
   (b) Patent : “應用於靜態記憶體之可容忍閘級崩毀之功率閘技術,” 中華民國專利申請案號:99134465。美國專利申請中。

計劃產出論文及專利表列。

(A) 3 Conferen Papers:

1. Hao-I Yang, Ching-Te Chuang, and Wei Hwang, "Impacts of Contact Resistance and NBTI/PBTI on SRAM with High-κ Metal-Gate Devices,” Proc. IEEE International Workshop on Memory Technology, Design, and Testing (MTDT), August 31-Sept. 2, 2009, Hsinchu, Taiwan, pp. 27-30.
2. Hao-I Yang, Ching-Te Chuang, and Wei Hwang, "Power-Switch Gate-Oxide Breakdown Tolerance Techniques for Power-Gated SRAM,” Proc. 2010 International Conference on IC Design and

Technology (ICICDT), Minatec in Grenoble, France, June 2-4, 2010, pp. 102-105.

3. Aditya Bansal, Rahul Rao, Jae-Joon Kim, Sufi Zafar, James H. Stathis, and Ching-Te Chuang, "Impact of NBTI and PBTI in SRAM Bit-cells: Relative Sensitivities and Guidelines for Application-Specific Target Stability/Performance," Proc. 2009 IEEE International Reliability Physics Symposium (IRPS), Montreal, Quebec, Canada, pp. 745-749. (with IBM).

(B) 4 Journal Paper:

1. Hao-I Yang, Wei Hwang, and Ching-Te Chuang, "Impacts of NBTI/PBTI and Contact Resistance on Power-Gated SRAM with High-κ Metal-Gate Devices," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, (accepted).
2. Hao-I Yang, Wei Hwang, and Ching-Te Chuang, "Impacts of Gate-Oxide Breakdown on Power-Gated SRAM," Microelectronics Journal, (accepted).
3. Hao-I Yang, Shyh-Chyi Yang, Wei Hwang, and Ching-Te Chuang, "Impacts of NBTI/PBTI on Timing Control Circuits and Degradation Tolerant Design in Nanoscale CMOS SRAM,"IEEE Transactions on Circuits and Systems – Part I: Regular papers (TCAS I), (under revision).
4. Aditya Bansal, Rahul Rao, Jae-Joon Kim, Sufi Zafar, James H. Stathis, and Ching-Te Chuang, "Impacts of NBTI and PBTI on SRAM Static/Dynamic Noise Margins and Cell Failure Probability", Journal of Microelectronics Reliability, Elsevier, vol. 49, 2009, pp. 642-649. (with IBM).

(C) 2 Patents:

1. 楊皓義, 莊景德, 黃威, 楊仕祺, "降低 NBTI/PBTI 效應於先進製程 SRAM 的寫入控制電路", 中華民國專利申請案號：098125793。美國專利申請中。
2. 楊皓義, 莊景德, 黃威, "應用於靜態記憶體之可容忍閘級崩毀之功率閘技術," 中華民國專利申請案號:99134465。 美國專利申請中。

附件二

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估 ■ 達成目標
2. 研究成果在學術期刊發表或申請專利等情形： 論文：■已發表 □未發表之文稿 □撰寫中 □無 專利：□已獲得 ■申請中 □無 技轉：□已技轉 □洽談中 ■無 其他：（以 100 字為限） 說明： **3** 篇國際學術會議論文(已發表) **4** 篇學術期刊論文: 已發表 (1), 接受 (2), 修改 (1) **2** 項專利: 降低 NBTI/PBTI 效應於先進製程 SRAM 的寫入控制電路”(案號：098125793); 應用於靜態記憶體之可容忍閘級崩毀之功率閘技術”(案號: 99134465)。

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以500字為限）

學術成就:

1. 分析 BTI 對不同應用(高效能或低功率)SRAM 的穩定度、存取速度、及良率的影響，並提出設計準則。

2. 分析 BTI 與接觸電阻在高電介質金屬閘極製程對採用功率閘的 SRAM 的穩定度及效能的影響；並提出可容忍　劣化效應的感測器。

3. 分析 BTI 對双埠 8T SRAM 穩定度、效能、速度、及時序控制的影響。此為第一篇討論到時序控制的論文。

4. 分析閘級崩毀對採用功率閘的 SRAM 的穩定度及效能的影響，並提出可容忍閘級崩毀之功率閘技術。

技術創新:

1. 降低 NBTI/PBTI 效應於先進製程 SRAM 的寫入控制電路”,專利申請案號：098125793, 98.07.31。美國(申請中)

2. 應用於靜態記憶體之可容忍閘級崩毀之功率閘技術,”專利申請案號:99134465，99.10.08。 美國(申請中)。

社會影響:

1. NBTI 侷限 PMOS 的微縮, 而 PBTI 嚴重影響高電介質金屬閘 NMOS。瞭解它們對 SRAM 的影響於半導體業界及晶圓代工廠之 SRAM Compiler 皆為當前重要課題。

2. 此計劃涵蓋數個領域，由元件物理、BTI 化學反應、劣化模型、到 SRAM 設計。訓練研究生瞭解、分析、及解決業界面對的真實挑戰。

附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99年06月24日

計畫編號	NSC 98－2221－E－009－112		
計畫名稱	奈米隨機存取記憶體的長時間可靠度劣化現象分析與可容忍此劣化現象之設計		
出國人員姓名	楊皓義	服務機構及職稱	國立交通大學電子工程學系(所)博士班研究生
會議時間	99 年 6 月 2 日至 99 年 6 月 4 日	會議地點	法國格勒諾柏
會議名稱	(中文)國際積體電路設計與技術會議 (英文) International Conference on IC Design & Technology		
發表論文題目	(中文)應用於靜態記憶體之可容忍閘級崩毀之功率閘技術 (英文)Power-Switch Gate-Oxide Breakdown Tolerance Techniques for Power-Gated SRAM		

一、參加會議經過

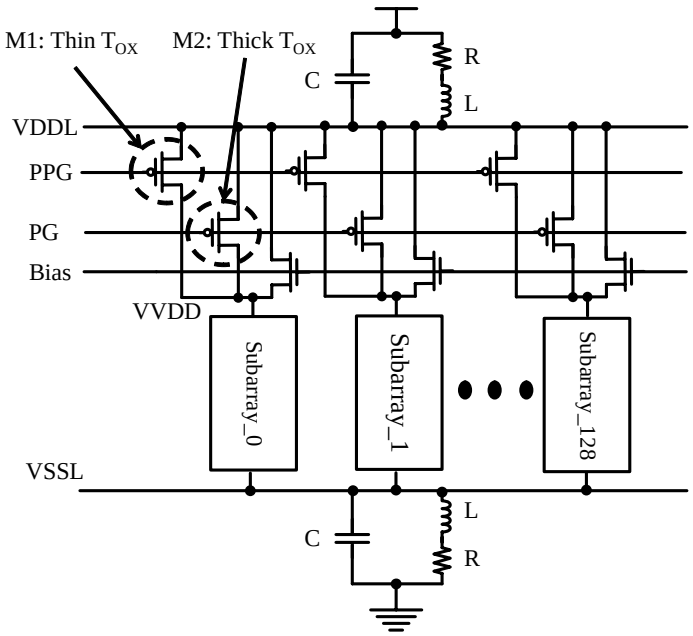
國際積體電路設計與技術會議希望藉由多個領域的共同研究，如先進積體電路設計、元件設計、設計工具與技術、與製程技術發展來加速產品上市時間，特別針對高速產品，其包含先進功率控制、漏電流控制、元件整合與良率控制。

此次國際積體電路會議在位於法國格勒諾柏首 MINATEC 舉行，會議時間為民國 99 年 6 月 2 日至民國 99 年 6 月 4 日；國際積體電路設計與技術會議為工程師、科學家、教授與學生提供了一個論壇，藉由在此論壇的互動，我們可以設計與製程技術，其有關產品、積體電路設計。此獨一的論壇包含了論文發表與特別的機會給技術者與產品設計者彼此互動，藉由彼此交換訊息來產生獨特的創意、突破性的想法、和充滿創造力

MINATEC 全景

的合作。兩天的技術發表會與意見交換論壇在一天的短期課程後舉行，短期課程提供許多有價值的訊息給有經驗的設計者與初學者。

第一天的短期課程包含為四場短期課程，包含【磁阻記憶體】，如何【減輕製程參數對邏輯設計的影響】,【3D 整合技術與 3D 積體電路】，與【預測與特性化製程參數變異】；【磁阻記憶體】與【3D 整合技術與 3D 積體電路】偏重於介紹與簡介而較少實用與設計方面的討論；【減輕製程參數對邏輯設計的影響】對於現在先進製程下的設計非常重要，並有容錯設計的討論；【預測與特性化製程參數變異】亦著重於因先進製程下導致設計參數變異對電路設計的影響。再接下來的第二天的會議中，包含先進記憶體、輸入輸出電路與靜電防護、先進電晶體與材料、系統單晶片與低功率、可靠度與電漿導致之損壞、3D 整合與電腦設計輔助介面；第三天的會議包括 DFM/DFT /DFR/DFY、高電壓/高功率、低功率、整合技術、Soft Error Rate 與高頻晶片與類比電路。



採用兩種不同閘極厚度之記憶體架構

我們的報告是在第二天會議的可靠度與電漿導致之損壞會議中進行，我們的會議論文名稱為【Power-Switch Gate-Oxide Breakdown Tolerance Techniques for Power-Gated SRAM】，論文內容為探討與設計功率閘來減輕或避免功率閘極崩毀，進而降低閘極崩毀對靜態隨機存取記憶體的影響。在論文中，我們闡述閘極崩毀已成為先進隨機存取記憶體設計上一個很大的挑戰，其中以功率閘的閘極崩毀對記憶體的穩定度影響最大；在我們的分析中，我們指出，當頭功率閘發生閘極崩毀後，靜態隨機存取記憶體的電壓遠將隨著的閘極崩毀愈嚴重而降低，進而導致靜態隨機存取記憶體的穩定度遭到破壞；相同的現象亦可在腳功率閘設計中發現，當腳功率閘發生閘極崩毀，隨機存取記憶體的接地端電壓將會上升，因而導致記憶體的穩定度下降。另外，當記憶體處與休眠狀況時，若頭功率閘發生閘極崩毀，則記憶體陣列的電壓源將上升，導致漏電流上升，功率閘結構失去其功用；相同的狀況亦可在腳功率上觀察到類似的狀況，當腳功率閘發生崩毀，記憶體陣列的接地端電壓將會下降，進而導致漏電流上升，功率閘亦

討論會場

喪失其功用。因此，我們提出在功率閘閘極與控制訊號輸出端之間插入一電阻藉此限定漏電流的發生，此方法雖然可以在當閘極崩毀很嚴重時有效地減少閘即漏電流，進而改善閘極崩毀對記憶體的影響，但當閘極崩毀不嚴重時，此方法卻會劣化記憶體的的雜訊邊界；另一種減輕功率閘閘極崩毀影響的方法即是避免閘極崩毀發生，電晶體發生閘極崩毀的時間與其閘極的電場有關，當閘級電場越高，則發生閘極崩毀的時間將會愈短，反之則越長，因此我們可利用閘極厚度較厚的電晶體或臨界電壓較高的電晶體做為功率閘來減少功率閘閘極崩毀發生的機會；但是閘極厚度較厚或臨界電壓較高的功率閘卻會導至記憶體會有較長的切換時間（從睡眠狀態到工作狀態），為了解決此問題，我們可以使用兩種不同閘極厚度或臨界電壓的電晶體功率閘，在此架構中，我們使用閘級較薄或臨界電壓較低的功率閘來做狀態切換，藉此維持切換速度，而在

海報張貼

工作狀態下，我們使用閘級較厚或臨界電壓較高的功率閘來提供記憶體電流，藉此可延長功率閘的壽命；此外，由於閘級厚度的改變對於電晶體壽命的影響較為明顯，因此論文中，我們較推薦改變閘級厚度的架構。

口頭報告結束後，我們亦有在論壇張貼海報進行討論，展示共計 60 分鐘。過程相當順利且很有收穫，在 poster 的過程中，雖然沒有人來與我們討論我們發表論文的問題，但可以跟參觀起他發表者的海報，藉此對其他領域有更進一步的了解，也可以知道自己不足的地方。另外使用英文跟不同國家的人交談，更可以加強自己的英文的聽和說的能力，整體的收獲算蠻豐富的。

二、與會心得

在此次會議中，除了參與短期課程外與發表論文外，亦有聆聽其他論文的發表，特別

藉由參與短期課程，聆聽有關目前容錯設計在克服製成飄移所產生的錯誤，使我們對於未來記憶體的架構設計有新的想法。

三、考察參觀活動(無是項活動者略)

無

四、建議

無

五、攜回資料名稱及內容

Proceeding (Soft and hard copy), Tutorial, 原子筆一支

六、其他

無

Power-Switch Gate-Oxide Breakdown Tolerance Techniques for Power-Gated SRAM

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ABSTRACT

The gate-oxide breakdowns (BD) of the power-switches have severe and even detrimental effects on the margin, stability, and performance of the power-gated SRAM. This paper proposes and evaluates several techniques to mitigate the power-switch gate-oxide BD, including adding a gate series resistance to the power switch, dual threshold voltage power switch, thick gate-oxide power switch, and dual gate-oxide thickness power switch. It is shown that dual gate-oxide thickness power switch improves the time-to-dielectric-breakdown of the power switch while maintaining the performance without side effect.

Index terms: gate-oxide breakdown, power gating technology, SRAM.

I. INTRODUCTION

With technology scaling, the gate-oxide thickness becomes thinner while the supply voltage remains relatively unchanged, leading to higher gate-oxide electric field and causing gate-oxide breakdown (BD). Gate-oxide breakdown has become a major concern in deep sub-100nm CMOS circuit designs. Besides, many state-of-the-art SRAM designs adopt dual-supply-voltage scheme, where peripheral circuits, such as decoders and sensing amplifiers, use the normal supply voltage to reduce power, and SRAM cell array uses the higher supply voltage, in order to maintain the cell stability. However, these schemes have a higher voltage across the cell array, thus increasing the probability of gate-oxide BD. Previous works have focused on the gate-oxide BD in the cell that degrades the already poor Static Noise Margin (SNM), Write Margin (WM) [1, 2], as well as the worst-case Read delay and leakage power [3]. Furthermore, most state-of-the-art SRAMs are designed with power-gating structures (Fig. 1) to reduce leakage in Standby or Sleep mode, and the power-switches suffer gate-oxide BD as well. The gate-oxide BDs of the power-switches have severe and even detrimental effects on the margin, stability, and performance of the SRAM array [4]. As such, we evaluate several techniques to mitigate the gate-oxide BD of the power-switch, including adding a gate series resistance to the power-switch, dual threshold voltage power-switch, thick gate-oxide power-switch, and dual-oxide thickness (dual T_{OX}) power-switch. Based on the evaluation results, the dual gate-oxide thickness power-gating structure is recommended. In Section II, we describe the details of our simulation model in PTM CMOS 32nm technology. The technique of adding a gate series resistance to the power-switch is analyzed in Section III. Section IV evaluates dual threshold voltage power-switch, thick gate-oxide power-switch, and dual gate-oxide thickness (dual T_{OX}) power-switch. The conclusion of the paper is given in Section V.

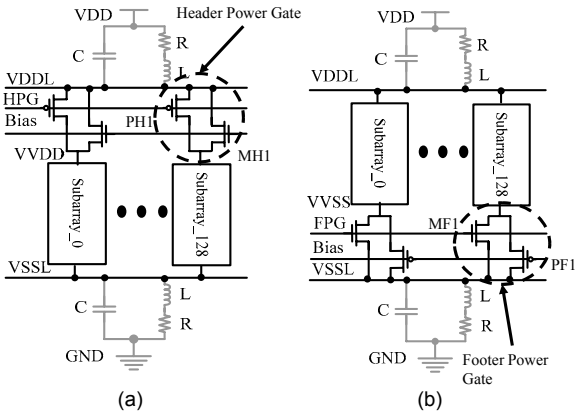


Fig. 1. Power-gated SRAM with (a) header, and (b) footer.

II. POWER-GATED SRAM MODELS

The post-BD characteristics of an NMOS can be explained by the location of a constant-size breakdown path and modeled as a narrow inclusion of highly-doped n-type silicon well with the equivalent circuit shown in Fig. 2 [5]. The equivalent post-BD resistance becomes smaller when the gate-oxide BD spot position is close to drain or source of a MOSFET (Fig. 3) [4]. The post-BD gate-to-drain and gate-to-source leakages affect SRAM most significantly. Thus, the model can reduce to simple equivalent resistance paths between the gate and source/drain under normal operating conditions. The gate leakage current after oxide hard BD can be modeled as I = (1/R)V; where V is the voltage across the gate-oxide, and R is the equivalent post-BD resistance

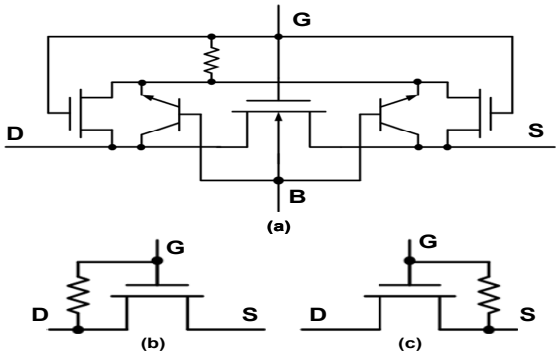


Fig. 2. (a) Equivalent gate-oxide HBD circuit model. This model can be simplified to (b) with gate-oxide HBD near drain, (c) with gate-oxide HBD near source [3].

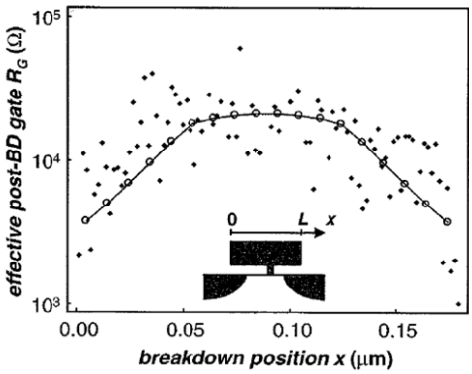


Fig. 3. Effective post-BD resistance vs. BD position [6].

depending on the BD spot area and its position.

SRAM power-gating structures can be classified into header- and footer-gating structures. Fig. 1(a) shows a column-based header-gated SRAM structure, wherein PH1 is the header power-switch, and MH1 is the clamping device to bias virtual supply (VVDD) for data retention in Standby/Sleep mode. Fig. 1(b) shows a column-based footer-gated SRAM structure. MF1 is the footer power-switch, and PF1 is the clamping device to bias virtual ground (VVSS) for data retention in Standby/Sleep mode. Package model [7] is also included in our analysis, and parasitic capacitance, inductance and resistance of the package are 5.32pF, 8.18nH, and 0.217Ω, respectively. The SRAM array size is 128x128 cells. The SRAM supply voltage is 0.9V, and the detailed analyzed results in the following sections are based on BSIM Predictive Model PTM 32nm [8].

III. Power Switch with a Gate Series Resistance

Previous work [4] has showed that the power-switch gate-to-drain BD degrades SRAM stability during Active mode and increase leakage power during Standby/Sleep mode. When power-switch gate-to-drain BDs happen, their leakage current paths discharge the voltage level of virtual supply rail (VVDD) in a header structure, and charge the voltage level of virtual ground (VVSS) in a footer structure. The VVDD (VVSS) may collapse during Active mode, leading to SRAM stability degradation. On the other hand, during Standby/Sleep mode, the gate-to-drain power-switch BD leakage current paths

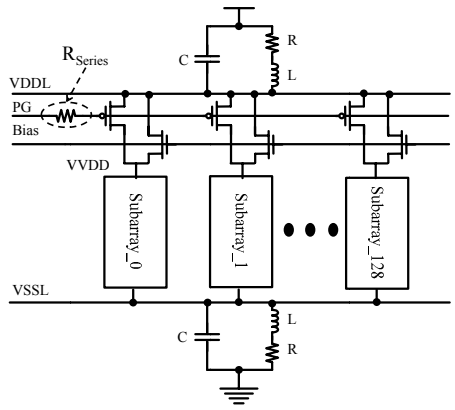


Fig. 4. A header-gated SRAM with R_{Series}.

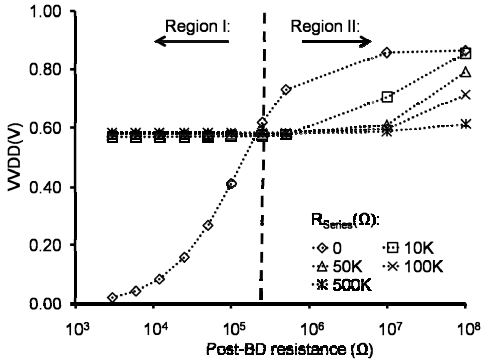


Fig. 5. Active mode VVDD vs. post-BD equivalent resistance when PHD BD happens.

charge the VVDD rail in a header structure, and discharge the VVSS voltage level in a footer structure, thus raising the voltage across the SRAM array and increasing the Standby/Sleep leakage/power.

To mitigate the gate-oxide BD and limit the leakage current through the gate-oxide of the power-switch, a series resistance, R_{Series}, could be added between the gate of the power-switch and its control signal, as shown in Fig. 4 for a header-gated structure. Fig. 5 shows the relation between VVDD and post header power-switch gate-to-drain BD (post-PHD BD) resistance with various values of R_{Series}. In Region I (post-PHD BD resistance smaller than $2.5\times10^5\Omega$) where the BD is serious, VVDD voltage level degradation is mitigated by using R_{Series} since it limits the post-BD leakage current. However, in Region II where the BD is mild to moderate, the VVDD voltage level decreases with R_{Series} inserted due to smaller V_{GS} of the power-switch caused by the voltage drop across R_{Series} (the gate voltage of power-switch increases as the post-BD leakage current flows through R_{Series}). Thus, the power-switch has less V_{GS} drive, and the voltage level of VVDD degrades. Fig. 6 shows the relations between RSNM and post-PHD BD resistance with various R_{Series}. Clearly, RSNM improves in Region I but degrades in Region II since RSNM depends on VVDD voltage level. To limit the gate-oxide BD leakage current of a footer power-switch, a series resistance can also be used in a footer-gated structure. The impacts on a footer-gated SRAM would be similar to a header-gated SRAM.

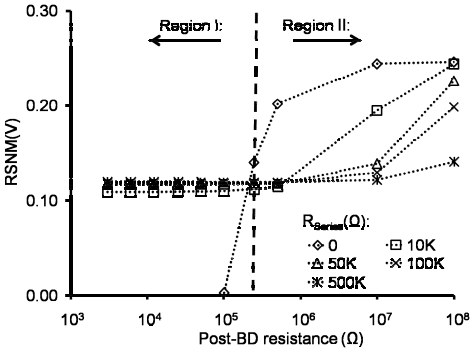


Fig. 6. RSNM vs. post-BD equivalent resistance in a header-gated SRAM with R_{Series} when PHD BD happens.

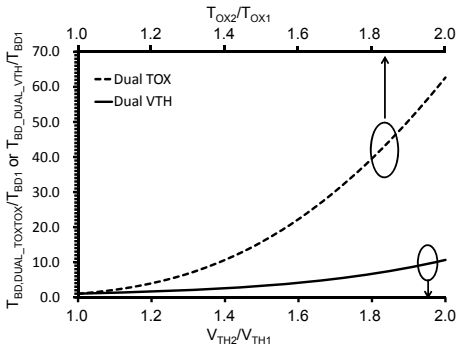


Fig. 7. T_{BD} ratio of NMOS devices with different V_{TH} or T_{OX} ratio.

IV. DUAL V_{TH} AND DUAL T_{OX} POWER-SWITCH

Another way to mitigate the impacts of power-switch gate-oxide BD is to prevent gate-oxide BD from happening. Time to breakdown (TBD) of gate-oxide can be formulated by Anode Hole Injection model [9] or Thermochemical model [10]. Conventionally, Anode Hole Injection model is used to describe gate-oxide T_{BD} at high gate-oxide field (E_{OX}), and Thermochemical model is used to describe gate-oxide T_{BD} at low E_{OX}. Because E_{OX} of our analysis model is in the low field region [11], we use Thermochemical model to calculate T_{BD} in our analysis. In Thermochemical model, T_{BD} can be formulated as:

$$T_{BD} \propto \exp\left(\frac{\Delta H_0}{k_B T} - \gamma E_{OX}\right) \quad (1)$$

,where ΔH_0 is the observed activation energy of the bond breakage, k_B is Botzmann constant, T is temperature, and γ is the field acceleration factor. According to Eq. (1), the T_{BD} ratio with different E_{OX} can be formulated as:

$$T_{BD2}/T_{BD1} = \exp\left[\gamma(E_{OX1} - E_{OX2})\right] \quad (2)$$

Moreover, the relation between E_{OX}, threshold voltage (V_{TH}), and gate-oxide thickness (T_{OX}) can be expressed as:

$$E_{OX} = \frac{V_{GS} - V_{TH}}{T_{OX}} \quad (3)$$

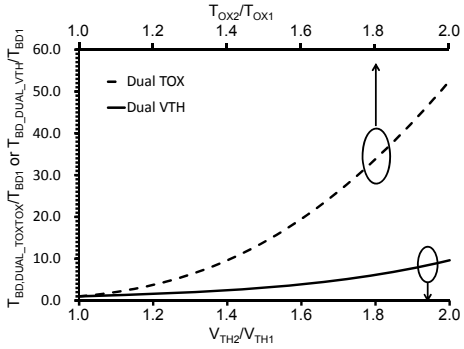


Fig. 8. T_{BD} ratio of PMOS devices with different V_{TH} or T_{OX} ratio.

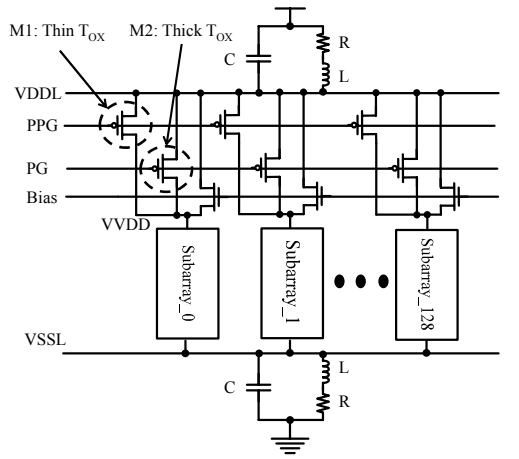
Therefore, the T_{BD} ratio with different T_{OX} and V_{TH} of NMOS and PMOS can respectively be formulated as:

$$T_{BD2}/T_{BD1} = \exp\left[\gamma\left(\frac{V_{GS} - V_{TH}}{T_{OX1}}\left(1 - \frac{T_{OX1}}{T_{OX2}}\right)\right)\right] \quad (4)$$

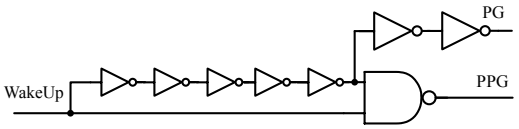
$$T_{BD2}/T_{BD1} = \exp\left[\gamma\left(\frac{V_{TH1}}{T_{OX}}\left(\frac{V_{TH2}}{V_{TH1}} - 1\right)\right)\right] \quad (5)$$

Fig. 7 and Fig. 8 show the T_{BD} ratio with different T_{OX} and V_{TH} of NMOS and PMOS respectively according to Eq. (4) and Eq. (5). Clearly, devices with higher V_{TH} or thicker T_{OX} have longer gate-oxide T_{BD}. Thicker T_{OX} devices offer better T_{BD} improvement than higher V_{TH} devices. Therefore, we can use higher V_{TH} devices or thicker T_{OX} devices to extend the life-time of power-switches and prevent gate-oxide BD from happening.

Although thick-T_{OX} power-switch and/or high-V_{TH} power-switches can prevent gate-oxide BD from happening, they degrade the wake-up transition performance. To resolve this problem, we propose a dual-T_{OX} power-gating structure and a dual-V_{TH} power-gating structure. In these structures, power switches with thick-T_{OX} (or high-V_{TH}) provide sufficient currents to SRAM array during Active mode, while power-switches with regular-T_{OX} (or regular-V_{TH}) are used to maintain SRAM wake-up performance. Moreover, according to Fig. 7, T_{BD} improvement by using high-V_{TH} is limited, and it may not be practical to increase V_{TH} to two times of regular V_{TH}. Hence, we focus on analyzing the dual T_{OX} power-gating structure. An example of our proposed dual-T_{OX} header-gating structure is shown in Fig. 9(a). In this structure, M1 is a thin gate-oxide device, and M2 is a thick gate-oxide device. Both of them serve as power-switches. During Sleep/Standby mode, both M1 and M2 turn off. During wake-up transition, M1 turns on first to charge up VVDD quickly, while M2 remains off. After VVDD voltage level approaches VDD, M1 turns off, and M2 turns on as SRAM enters Active mode. In Active mode, M1 remains off while M2 remains on to provide sufficient current to the SRAM cell array. Fig. 9(b) shows the timing control circuit for signals PPG and PG of M1 and M2. By using inverter chain delay, PG becomes "logic 0" right after PPG becomes "logic 1". Fig. 10 compares pertinent waveforms and wake-up currents during wake-up transition for three different header-gating structures: namely,



(a)



(b)

Fig. 9. (a) A dual-TOX header power-gating structure, and (b) timing control circuit for signals PPG and PG of M1 and M2.

single regular gate-oxide power-switch, single thick gate-oxide power-switch, and dual gate-oxide power-switch. In our analysis, the thick T_{OX} (T_{OX2}) is twice the thickness of the regular T_{OX} (T_{OX1}). We also maintain the same W/L ratio for both power-switch devices in the dual-T_{OX} power-gating structure as that of the power-switch device in the single T_{OX} power-gating structure. As can be seen in Fig. 10, the wake-up transition performance of dual-T_{OX} power-gating structure is comparable to the case with single regular T_{OX} power-switch. In contrast, the use of single thick T_{OX} header significantly degrades the wake-up transition performance. Finally, according to Fig. 8, T_{BD} of dual-T_{OX} header can be extended to about 51 times the T_{BD} of the single regular T_{OX} case. Notice that thick T_{OX} device typically requires longer channel length in order to contain the short channel effect. The area overhead of the proposed dual-T_{OX} power-gating structure depends on the organization and partition of the overall power-gating structure, and should not be significant compared with the SRAM cell array area.

V. CONCLUSIONS

We have proposed several techniques to mitigate the impacts of power-switch gate-oxide BD on SRAM. Adding a gate series resistance to the power-switch could improve the SRAM stability and decrease leakage power when power-switch gate-oxide BD is serious. However, when power-switch gate-oxide BD is mild or moderate, this technique degrades the SRAM stability. We evaluated and compared proposed dual threshold voltage power-switch, thick gate-oxide power- switch, and dual gate-oxide thickness power-switch to prevent gate-oxide BD from happening. Based on the evaluation results, we recommended the dual-T_{OX} power-gating structure as this technique was most effective in

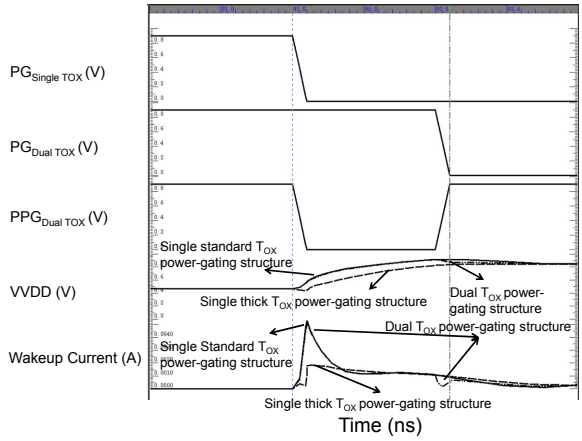


Fig. 10. Pertinent waveforms and wake-up currents during wake-up transition for three different header-gating structures: single regular gate-oxide power-switch, single thick gate-oxide power-switch, and dual gate-oxide power-switch.

extending the life-time of power-switches while maintaining the wake-up performance.

ACKNOWLEDGEMENT

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國科會補助計畫衍生研發成果推廣資料表

日期:2010/11/02

國科會補助計畫	計畫名稱：奈米隨機存取記憶體的長時間可靠度劣化現象分析與可容忍此劣化現象之設計
	計畫主持人：莊景德
	計畫編號：98-2221-E-009-112- 學門領域：積體電路及系統設計

無研發成果推廣資料

98 年度專題研究計畫研究成果彙整表

計畫主持人：莊景德	計畫編號：98-2221-E-009-112-
計畫名稱：奈米隨機存取記憶體的長時間可靠度劣化現象分析與可容忍此劣化現象之設計	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	2	2	70%	件	(1) 楊皓義, 莊景德, 黃威, 楊仕祺, ’降低 NBTI/PBTI 效應於先進製程 SRAM 的寫入控制電路’, 中華民國專利申請案號：098125793, (2) 楊皓義, 莊景德, 黃威, ’應用於靜態記憶體之可容忍閘級崩毀之功率閘技術,’中華民國專利申請案號:99134465.
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	2	2	70%	人次	
		博士生	1	1	70%		
		博士後研究員	0	0	100%		
		專任助理	0	0	20%		
國外	論文著作	期刊論文	3	4	70%	篇	4 篇國際學術期刊論文：J. Microelectronics Reliability (appeared), IEEE TVLSI (accepted), Microelectronics Journal (accepted), IEEE TCAS (under revision)

		研究報告/技術報告	0	0	100%		
		研討會論文	3	3	70%		3 篇國際學術會議論文： IRPS'09, MTDT'09, ICICDT'09
		專書	0	0	100%	章/本	
	專利	申請中件數	1	2	70%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)		Ching-Te Chuang and Pin Su, Invited Talk ' Variability and Design of SRAM in Scaled and Emerging Technologies, ' 1st IEEE International Variability Characterization Workshop, Hsinchu, Taiwan, April 30, 2010.					

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 ■申請中 □無

技轉：□已技轉 □洽談中 ■無

其他：（以 100 字為限）

3 篇國際學術會議論文(已發表)

4 篇學術期刊論文: 已發表 (1), 接受 (2), 修改 (1)

2 項專利: 降低 NBTI/PBTI 效應於先進製程 SRAM 的寫入控制電路’（案號：098125793）；應用於靜態記憶體之可容忍閘級崩毀之功率閘技術’（案號: 99134465）。

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以500字為限）

學術成就:

1.分析 BTI 對不同應用(高效能或低功率)SRAM 的穩定度、存取速度、及良率的影響，並提出設計準則。

2.分析 BTI 與接觸電阻在高電介質金屬閘極製程對採用功率閘的 SRAM 的穩定度及效能的影響；並提出可容忍 劣化效應的感測器。

3.分析 BTI 對双埠 8T SRAM 穩定度、效能、速度、及時序控制的影響。此為第一篇討論到時序控制的論文。

4.分析閘級崩毀對採用功率閘的 SRAM 的穩定度及效能的影響，並提出可容忍閘級崩毀之功率閘技術。

技術創新:

1. 降低 NBTI/PBTI 效應於先進製程 SRAM 的寫入控制電路’,專利申請案號：098125793, 98.07.31。美國(申請中)

2. 應用於靜態記憶體之可容忍閘級崩毀之功率閘技術,’ 專利申請案號:99134465，99.10.08。 美國(申請中)。

社會影響:

1. NBTI 侷限 PMOS 的微縮, 而 PBTI 嚴重影響高電介質金屬閘 NMOS。瞭解它們對 SRAM 的影響於半導體業界及晶圓代工廠之 SRAM Compiler 皆為當前重要課題。

2. 此計劃涵蓋數個領域，由元件物理、BTI 化學反應、劣化模型、到 SRAM 設計。訓練研究生瞭解、分析、及解決業界面對的真實挑戰。