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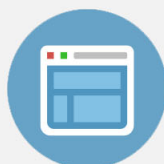
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# Speed control of the 12-step sensorless drive for a brushless dc motor

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The 12-step sensorless drive scheme requires an interval to detect the zero crossing of the back emf. The voltage regulating pulse-width modulation (PWM) is commonly used for the speed control of a motor. However, it induces the fluctuation of the back emf and makes the zero-crossing detection difficult. This paper proposes two digital approaches to the zero-crossing detection for the presence of the PWM. One approach is to vary the zero-crossing detecting period linearly with respect to the speed of the motor. The other is to detect the back emf only on the positive pulses of the PWM in order to avoid the fluctuation of the back emf. A digital filter is also incorporated in order to eliminate the noise generated by the PWM. Experiments show that both approaches have good performance for the speed control of the brushless dc motor. © 2008 American Institute of Physics. [DOI: 10.1063/1.2838230]

## I. INTRODUCTION

Recently, several sensorless drive schemes have been proposed for a brushless dc motor.<sup>1–3</sup> Among them, Wang *et al.*<sup>3</sup> presented a novel 12-step sensorless drive scheme for a three-phase brushless dc motor, so that the active angular period can be extended from 120° to 168.75°. It has been shown that the larger the active angular period is, the larger is the torque generated by the motor. However, the detecting period for the zero crossing is fixed to 30 electrical degrees in the 12-step sensorless drive scheme. It results in the difficulty for the speed control of the motor, especially for low speed, since the duty cycle of the pulse-width modulation (PWM) in the zero-crossing detecting period must be full. Shao *et al.*<sup>4</sup> presented analog circuit for the back emf detection in the presence of the PWM.

To overcome this problem, this paper proposes two digital approaches to the zero-crossing detection for the presence of the PWM. The first approach is to vary the zero-crossing detecting period linearly with respect to the speed of the motor. When the speed is slower, the electrical angle range for the zero-crossing detection shrinks, so that the time period for the zero-crossing detection is still almost the same for different speeds. Thus, the performance of the detection is not affected, while the PWM can work for a wide range of speeds.

An alternative approach is to detect the back emf only on the positive pulses of the PWM in order to avoid the fluctuation of the back emf. Such an approach can be easily implemented by a field-programmable gate array (FPGA) chip. Moreover, it requires additionally a digital filter to eliminate the noise generated by the PWM.

## II. 12-STEP SENSORLESS DRIVE

For simplicity, this paper considers only the 12-step 150° sensorless drive scheme, which combines the 120° and 180° drives. Between the electrical angles of  $(30+60k)$  and  $(60+60k)$  degrees, where  $k$  is a natural number, the motor rotates in the six-step 120° drive mode so that the zero-crossing points can be detected, while the 180° drive mode applies between the electrical angles of  $(0+60k)$  and  $(30+60k)$  degrees. This is illustrated in Fig. 1. It is apparent that there are 12 steps in an electrical circle. The odd steps are the 180° drive mode, while the even steps are the 120° drive mode. It can also be seen in Fig. 1 that it lasts 150 electrical degrees before changing the polarity of one phase. There are two phase commutations for each zero crossing of the back emf:

- One is at the same time of the happening of the zero crossing (for the 180° drive mode) and
- The other is  $T_{ZC}(k)/2$  delay (for the 120° drive mode),

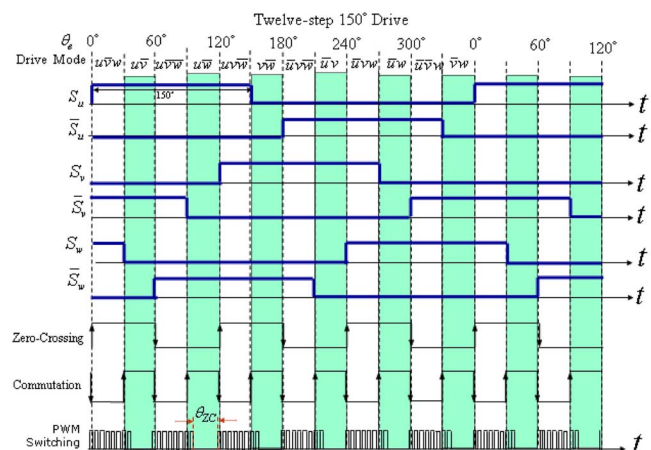


FIG. 1. (Color online) 12-step 150° sensorless drive scheme.

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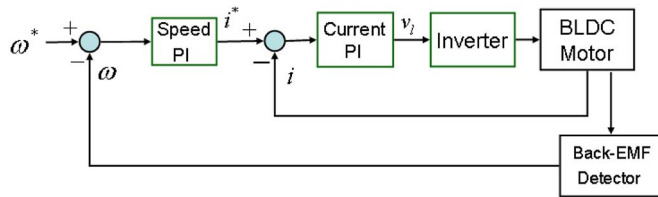


FIG. 2. (Color online) Speed control block diagram of a BLDC motor.

where  $T_{ZC}(k)$  is the interval time between the  $(k-1)$ th and the  $k$ th zero-crossing points of the back emf.

For the speed control, the dc load voltage is regulated by a switching transistor driven by a PWM signal, so that the load voltage is proportional to the duty cycle of the PWM. In Ref. 3 the zero-crossing detection period is fixed to be 15 electrical degrees. A direct extension to the speed control is to set this period having full duty cycle of the PWM, so that the zero-crossing detection is not affected by the PWM. However, low speed control will fail, since the dc load voltage is only partly controlled and is equal to the supply voltage in the detection period.

### III. VARYING-PERIOD APPROACH

Let  $\theta_{ZC}$  be the angular period of the zero-crossing detection (see Fig. 1). First, the motor runs with the full duty cycle of the PWM and  $\theta_{ZC}=15^\circ$  to obtain the possible maximum speed  $v_M$ . Next, set the duty cycle as the unit duty cycle

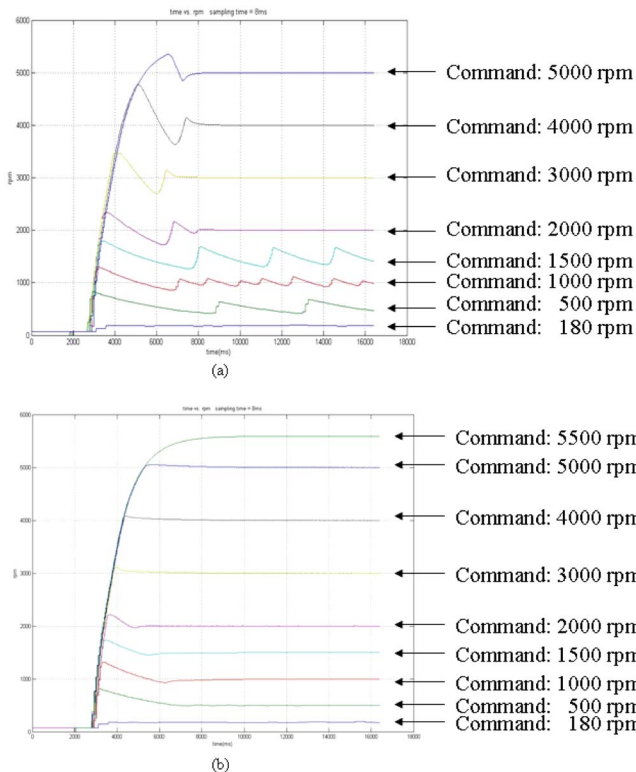


FIG. 3. (Color online) Speed responses for the varying-period zero-crossing detection: (a) without the antiwindup; (b) with the antiwindup.

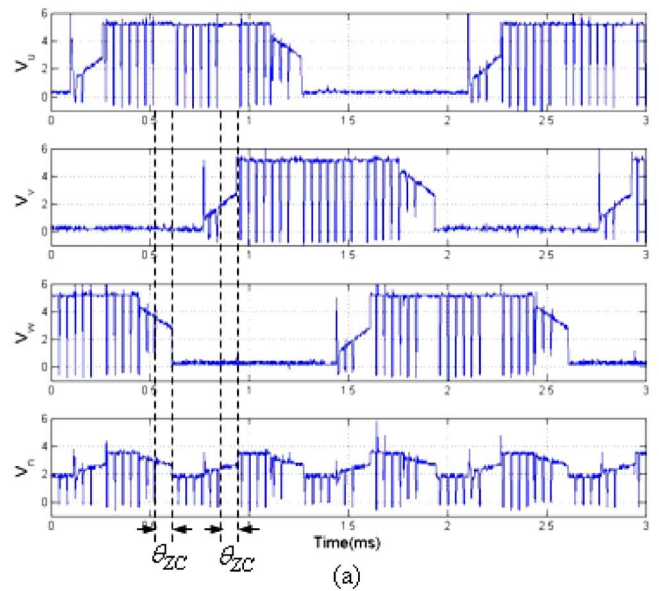


FIG. 4. (Color online) Voltage histories of the three phases for the varying-period zero-crossing detection: (a) 5000 rpm; (b) 1000 rpm.

(e.g.,  $2^{-11}\%$ ) and  $\theta_{ZC}=1^\circ$  to achieve the possible minimum speed  $v_m$ . The linearly varying-period relation of  $\theta_{ZC}$  to the speed  $v$  is then

$$\theta_{ZC} = 1^\circ + \frac{15^\circ - 1^\circ}{v_M - v_m}(v - v_m). \quad (1)$$

Two cascade proportional integral (PI) controllers form the speed control scheme of the motor with the 12-step  $150^\circ$  sensorless driver, as shown in Fig. 2. The inner PI loop is for the current control and is incorporated with an antiwindup strategy. Its output  $v_i$  generates the duty cycle of the PWM. The antiwindup PI controller can be written as<sup>5</sup>

$$v_i = v_l + K_{ci}e_i t_s + K_{cp}(e_i - i_a), \quad (2)$$

where  $e_i = i - i^*$ ,  $t_s$  is the sampling time and  $i_a$  is the output of the antiwindup. The compensation value  $i_a$  is the result of

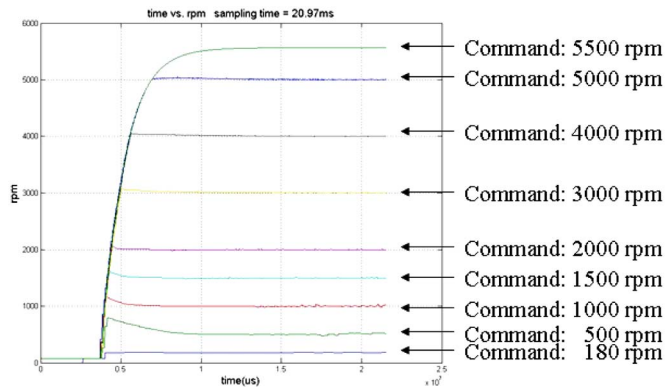


FIG. 5. (Color online) Speed responses for the zero-crossing detection with the digital filter.

multiplying the excess of  $v_l$  over the saturation limit (e.g.,  $2^{11}$ ) with the gain  $K_a$ .

A brushless dc (BLDC) motor used as a spindle motor of a  $50\times$  CD-ROM is taken as an experimental target. The speed control algorithm is implemented on an FPGA chip with 50 MHz. The carrier frequency of the PWM is set as  $50/2^{11}=0.0244$  MHz. It is found that  $v_M=5500$  rpm and  $v_m=180$  rpm. The histories of the speed responses without and with the antiwindup are shown in Fig 3. The responses for the controller without the antiwindup have fluctuations, especially for low speed commands. This is because the outputs of the controller touch the bound several times. On the contrary, the controller with the antiwindup has very good performance. It is also verified that the linearly varying zero-crossing detection period is effective for the speed control. Figure 4 shows, furthermore, the voltage histories of the three phases for the speed commands of 5000 and 1000 rpm. It is easy to see the full duty cycle intervals for the zero-crossing detection;  $14.1^\circ$  for 5000 rpm and  $3.6^\circ$  for 1000 rpm.

#### IV. DIGITAL FILTER APPROACH

The approach without interrupting the PWM signals is to detect the back emf only on the positive pulses of the PWM. This approach is hard to implement on a DSP or a microprocessor; but is easy on an FPGA chip, since a FPGA handles all processes including the PWM in the pace of the system clock. This approach utilizes the following techniques:

- A synchronization mechanism with the PWM provides the start and the end of each positive pulse of the PWM. The zero-crossing detection is performed only in the intervals of the positive pulses.
- Two stages of digital filter are applied. One is a delay of two system clocks from the start of a positive pulse before detecting the zero crossing. The other stage is a noise elimination filter, which records consecutive results of the comparator of the back emf with the neutral voltage for five system clocks. If five consecutive results are all true, the zero crossing occurred five system clocks ago.

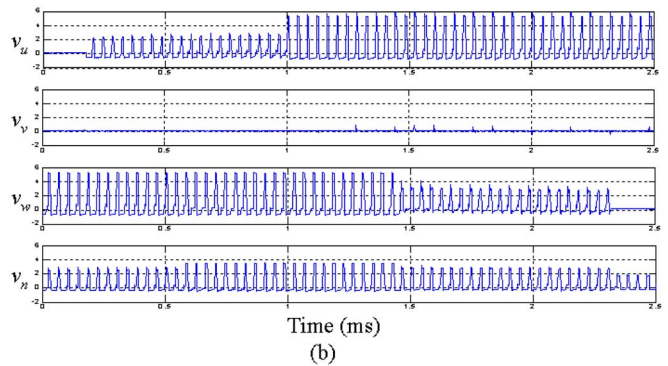
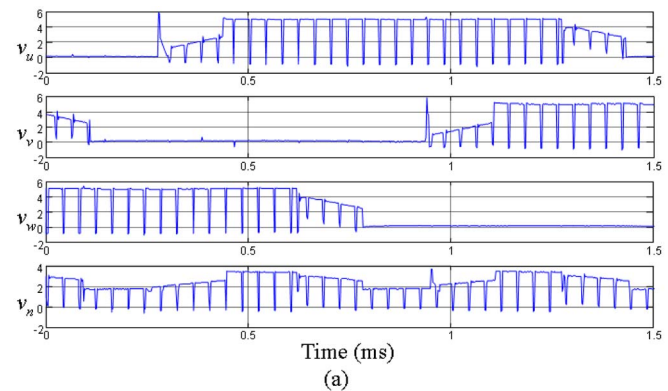


FIG. 6. (Color online) Voltage histories of the three phases for the zero-crossing detection with the digital filter: (a) 5000 rpm; (b) 1000 rpm.

The histories of the speed responses with the digital filter for the zero-crossing detection are shown in Fig. 5. It is of no doubt that the resulting performance is satisfied. The overshoots are even a little less than those in the varying-period approach. The voltages of the three phases are recorded in Fig. 6, which show that there are some noises in the positive pulses.

#### V. CONCLUSIONS

This paper proposes two digital approaches to the zero-crossing detection for the presence of the PWM. An antiwindup PI speed controller incorporated with one of these two approaches has been proved well suitable for the speed control of a BLDC motor with the 12-step sensorless driver. Experimental results also show the voltage behaviors of the three phases during the speed control.

#### ACKNOWLEDGMENTS

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