

行政院國家科學委員會專題研究計畫 期中進度報告

異質接面電晶體的安全操作範圍研究(1/2) 期中進度報告(精簡版)

計畫類別：個別型

計畫編號：NSC 94-2215-E-009-060-

執行期間：94年08月01日至95年07月31日

執行單位：國立交通大學電子工程學系及電子研究所

計畫主持人：李建平

處理方式：本計畫可公開查詢

中 華 民 國 96年09月13日

行政院國家科學委員會專題研究計畫成果報告

異質接面電晶體的安全操作範圍研究(1/2)

Investigation of safe operating area of an HBT

計畫編號：NSC 94-2215-E-009-060

執行期限：94 年 8 月 1 日至 95 年 7 月 31 日

主持人：李建平教授 國立交通大學電子工程學系

計畫參與人員： 國立交通大學電子工程學系

一、中文摘要

本研究探討自熱效應與崩潰效應對砷化鎵異質接面電晶體的安全工作區域的影響，可推導出一組簡單且解析的方程式用以描述上述兩效應對安全工作區域的影響，柯克（Kirk）效應所導致的崩潰現象（KIB）可用以解釋在高電流操作時的崩潰電壓下降，如果元件有合適的射極壓艙電阻，則主要是由 KIB 效應則決定元件高電流操作區的故障機制，而熱效應則決定低電流操作區的故障機制。

關鍵詞：安全工作區、異質接面電晶體（HBT）、柯克（Kirk）效應、自熱效應、砷化鎵

Abstract

The safe operating area (SOA) of GaAs based heterojunction bipolar transistors has been studied considering both the self-heating effect and the breakdown effect. Simple and analytical equations are derived to describe these two effects on SOA. The kirk effect induced breakdown (KIB) was considered to account for the decrease of the breakdown voltage at high currents. With reasonable emitter ballastors, the KIB effect was shown to be the major cause for device failure at high currents, while the thermal effect controls the low current failure.

Keywords: Safe operating area, Heterojunction bipolar transistor (HBT), Kirk effect, Self-heating effect, GaAs

Introduction

GaAs based heterojunction bipolar transistors (HBTs) have long been recognized as the leading device technology for high speed high power applications. With the increased popularity of wireless communications, extending the HBTs' capability into even higher power for base station applications is quite obvious. To significantly increase the power handling capability, the devices need to be operated at voltages much higher than what is normally used today. We have recently demonstrated a 28V InGaP/GaAs power HBT with high efficiency and high linearity. [1] The BV_{cbo} of the transistors was beyond 70 V. Kurpas et. al have also reported InGaP HBTs with high voltage capabilities.[2] The advantages of using InGaP HBTs over traditional LDMOSs include better efficiencies, higher operating frequencies and better linearity.

Thermal effect induced breakdown and its effect on SOA

HBTs, as in all bipolar devices, suffer from various feedback phenomena, which may cause instability and device failure in certain operating conditions. The most well known damaging effect is the “thermal runaway” caused by self-heating. [3-8] When a bipolar transistor is operated at high powers, the increased junction temperature causes the bandgap energy and therefore the emitter junction built-in potential to drop. As a result, the collector current increases. An approximate expression for the collector current under such electro-thermal feedback can be shown as

$$I_c = I_0 \exp\left[\frac{q}{kT}(V_{be} - R_e I_e - R_b I_b + R_{th} \phi I_c V_{ce})\right] \quad (1)$$

where R_{th} is the thermal resistance and ϕ is the electro-thermal feedback coefficient, typically $1.25\text{mV}/^\circ\text{C}$ for GaAs. At high power operations, the I_c - V_{be} curve can bend backwards at high currents. Once the device hits the bend-over point, it can have two solutions for its I - V characteristics and therefore causing device instability. If there are multiple fingers, some of the fingers may go into the high current state and some into low current state causing the hot fingers to thermally run away. A simple way to alleviate this problem is to increase R_e , or to add ballast resistors. [9-12] The instability can then be delayed to higher currents. In normal operations where I_b is much smaller than I_e , the instability (or SOA) boundary is defined by, according to Eq.(1),

$$I_c = \frac{kT/q}{R_{th}\phi V_c - R_e} \quad (2)$$

Kirk effect induced breakdown and its effect on SOA

For transistors operated at high voltages, another effect that is even more devastating can happen. That is the impact ionization or avalanche effect. When this happens in the collector, for an NPN transistor, the avalanche current results in a hole current back injected into the base. [13-17] This current can reverse the sign of the base current, so the third term in Eq.1 behaves similarly to the self-heating effect. It causes V_{be} to drop and leads to device instability. This impact ionization caused instability can be much worsened when Kirk effect happens. For transistors with high BV_{cbo} 's, the collector doping is usually low. When the injected carrier density exceeds the doping density, Kirk effect takes place and the location of the peak electric field shifts from the base-collector interface to the collector-subcollector interface. If the collector voltage is high enough, avalanche breakdown happens. Because the space charge concentration in the collector is now $\frac{J_c}{qV_s} - N_d$, which increases with the current flowing through the collector, the impact ionization and avalanche breakdown will take place at a lower voltage as the current increases. The additional base current caused by the avalanche process can provide a feedback mechanism resulting in device failure.

This mechanism can be seen clearly from the following expression for the collector current under breakdown condition,

$$I_c = \alpha M I_0 \exp\left[\frac{q}{kT}(V_{be} - R_e I_e - R_b I_b^* + R_{th} \phi I_c V_{ce})\right] \quad (3)$$

where α is the common base current gain and M is the avalanche multiplication factor. Notice the base current, I_b^* , now includes the hole current flowing back to the base terminal due to the impact ionization in the collector. Since the avalanche current is in the reverse direction of the normal base current, the voltage drop across the base resistance will change sign when the back injected hole current is higher than the normal base current. So this base resistance voltage drop serves as a positive feedback for the collector current in the same way as the self-heating effect. So under this situation, the device will also be killed.

The commonly used expression for the multiplication factor is

$$M = \frac{1}{\left(1 - \frac{V_{bc}}{BV_{cbo}}\right)^n} \quad (4)$$

Because of the Kirk effect, BV_{cbo} needs to be changed to the breakdown voltage, BV_{KIB} , with the presence of the collector current. Since the effective space charge concentration changes sign and increases with the current because of the Kirk effect, this new breakdown voltage, BV_{KIB} , decreases as the collector current increases. So the onset voltage of instability decreases with the current. For transistors with low collector doping, as in most high voltage transistors, the Kirk effect induced breakdown (KIB) becomes the major cause for device failure at high currents. This breakdown caused device failure is much more important than the thermal effect when devices are under RF operation. The thermal effect has a very long time constant, so it does not show up easily when devices are operated at high frequencies. But the breakdown effect is nearly instantaneous, the device will be killed immediately when the device's operating point hits the unstable point.

Therefore, in order to define the safe operating area (SOA) of an HBT, one has to consider both the thermal effect and the KIB effect. In the I_c - V_{ce} plane, the SOA boundary defines the region that the device can be safely operated. Once the device's operating point hits the SOA boundary, two solutions will result leading to device failure. After understanding the cause for device instability, the SOA boundary can be solved by searching for the unstable points using eqs. (1), (3), (4). To account for the effect of the terminal resistors, which are important in the feedback effects mentioned above and when external ballast resistors are used, the terminal voltages are adjusted to include all the voltage drops across the resistors. Since BV_{KIB} depends on the current injected into the collector because of KIB, BV_{KIB} as a function of the current has to be determined before the equations can be solved. It should be mentioned that this current is only the current injected from the emitter, the current from the avalanche process, which generates equal amount of electrons and holes, should not be included. In this study, BV_{KIB} 's under different current injection conditions are calculated using a one-dimensional semiconductor device simulator "SimWindows".[18] The effective space charge concentration in the collector is taken to be $N_d(x) - J/qv_s$, where $N_d(x)$ is the

collector's doping density and v_s is the electron's saturation velocity. The breakdown is defined when the peak electric field reaches the critical breakdown field. We have compared this calculation with the more elaborate calculation using electron/hole impact ionization rates. The results are very close to each other.

Representations of SOAs

The mutually dependent Eqs 1-4 were solved for the device I-V characteristics. Temperature dependences of the current gain and the thermal resistance were taken from experimental results and were considered in the calculation. The solved device characteristics are best described by a three-dimensional plot in the I_c - V_{be} - V_{ce} space. Any two variables are enough to determine the device's operation point in this space. All the allowed solutions are therefore represented by a surface in the 3-D plot. Here we take an example of an InGaP/GaAs NPN HBT with a collector thickness of 2.5 μm , which is uniformly doped to a doping concentration of $6 \times 10^{15} \text{cm}^{-3}$. The emitter size was assumed to be $3 \times 8 \mu\text{m}^2$, the emitter resistance (including ballastor), base resistance and collector resistance were taken to be 50 ohm, 17 ohm and 2 ohm, respectively. The calculated I-V characteristics are shown in Fig. 1. The X and Y axes are taken as V_{ce} and I_c while the Z axis is V_{be} . This mountain-shaped surface represents the allowed operation points for the device. The mountain ridge, which runs from the high I_c , low V_{ce} corner to the low I_c , high V_{ce} corner, is the local maximum for V_{be} and is the dividing line for the device's safe operation and unstable operation. We can picture this as follows: if we bias the device with certain V_{ce} and slowly increase the collector current, the V_{be} value goes up until it reaches the ridge of the mountain. At this point, V_{be} can no longer go any higher. If we let V_{be} go down, there are two paths for the device to go down hill. In other words, there will be two solutions, one with a higher current and the other with a lower current once the device passes the ridge. So the device fails if its operation reaches the ridge. This ridge, which is a curve in our 3-D space, is therefore the SOA (safe operation area) boundary. The projections of the curve onto the $I_c - V_{ce}$, $I_c - V_{be}$ and $V_{be} - V_{ce}$ planes are the different representations of the SOA boundary in different coordinate systems. The calculated SOA boundary and its representations in the three planes for our example are shown in Fig.2.

Since the SOA is usually shown as a curve in the $I_c - V_{ce}$ plane, we focus our following discussions on the representation on this plane. (however we need to bear in mind that the real curve should be in a 3-D space) First we did a set of calculations with constant V_{be} inputs of 1.25V, 1.3V, 1.4V, 1.5V and 1.6V. The calculated I-V curves are shown in Fig.3. For each curve there is a bend-over point, beyond which the device becomes unstable because each V_{ce} / V_{be} pair gives two solutions. The connection of all the bend-over points is the SOA boundary, which is the same as the projection of the 3-D SOA curve on the $I_c - V_{ce}$ plane.

References:

1. N. L. Wang, W. Ma, S. Xu, E. Camargo, X. Sun, P. Hu, Z. Tang, H. F. Chau, A. Chen, and C.P. Lee, "28V High-Linearity and Rugged InGaP/GaAs Power HBT", 2006 IEEE International Microwave Symposium, San Francisco, CA
2. P. Kurpas, A. Maaßdorf, W. Doser, W. Köhler, P. Heymann, B. Janke, F. Schnieder, H. Blanck, P. Auxemery, D. Pons, W. Heinrich, J. Würfl, "Power GaInP/GaAs HBTs for High Voltage Operation", The 2003 International Conference on Compound Semiconductor Manufacturing Technology (GaAs MANTECH), Scottsdale, AZ, paper 5.5
3. R. H. Winkler, "Thermal properties of high power transistors", *IEEE Tran. Elec. Device.*, vol. ED-14, no. 5, pp. 260-264, 1967
4. L. L. Liou, B. Bayraktaroglu and C. I. Huang, "Thermal instability analysis of multiple-finger microwave AlGaAs/GaAs heterojunction bipolar transistors", *IEEE MTT-S Microwave Symp. Tech. Dig.*, p. 281, 1993
5. W. Liu, S. Nelson, D. Hill, and A. Khatibzadeh, "Current gain collapse in microwave multi-finger heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 40, pp. 1917-1927, Nov. 1993.
6. W. Liu and A. Khatibzadeh, "The collapse of current gain in multi-finger heterojunction bipolar transistors: its substrate temperature dependence, instability criteria and modeling", *IEEE Trans. Electron Devices*, vol. 41, pp. 1698-1707, Oct. 1994.
7. Y. Zhu, J. K. Twynam, M. Yagura, M. Hasegawa, T. Hasegawa, Y. Eguchi, Y. Amano, E. Suematsu, K. Sakuno, N. Matsumoto, H. Sato, and N. Hashizume, "Self-heating effect compensation in HBTs and its analysis and simulation," *IEEE Trans. Electron Devices*, vol. 48, pp. 2640-2646, Nov. 2001.
8. N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: part I – single-finger devices", and "part II- two finger devices" *IEEE Trans. Electron Devices*, vol. 52, pp. 2009-2021 and pp. 2022-2033 Sep. 2005
9. G. B. Gao, M. S. Unlu, H. Morkoc, and D. L. Blackburn, "Emitter ballasting resistor design for the current handling capability of AlGaAs/GaAs power heterojunction bipolar transistors", *IEEE Trans. Electron. Device.*, vol.38, no.2, pp. 185-196, 1991
10. C. H. Liao, C. P. Lee, N. L. Wang, and B. Lin, "Optimum design for a thermally stable multifinger power transistor," *IEEE Trans. Electron Devices*, vol. 49, pp. 902-908, May 2002.
11. C. H. Liao and C. P. Lee, "Optimum Design for a Thermally Stable Multi-finger Power Transistor with Temperature dependent thermal conductivity", *IEEE Trans. Electron Device*, vol. 49, pp. 909-915, 2002
12. W. Liu, A. Khatibzadeh, J. Sweder, and H. Chau, "The use of base ballasting to prevent the collapse of current gain in AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 43, pp. 245-251, Feb. 1996.
13. J. D. Hayden, D. Burnett, and J. Nangle, "A comparison of base current reversal and bipolar snapback in advanced n-p-n bipolar transistors", *IEEE Electron Device Lett*, vol. 12, pp. 407-409, Aug 1991
14. G. Verzellesi, G. Baccarani, C. Canali, P. Pavan, L. Vendrame, and E. Zanoni, "Prediction of impact-ionization-induced snap-back in advanced Si n-p-n BJT's by means of a nonlocal analytical model for the avalanche multiplication factor", *IEEE Trans. Electron Devices*, vol. 40, pp. 2296-2300, Dec. 1993

15. M. Rickelt, H.-M. Rein and E. Rose, "Influence of impact-ionization-induced instabilities on the maximum usable output voltage of Si-bipolar transistors", *IEEE Trans. Electron Devices*, vol. 48, pp. 774-783, April 2001
16. T. Vanhoucke and G. A. M. Hurkx, "Unified electro-thermal stability criterion for bipolar transistors", 2005 IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM2005), pp.37-40.
17. N. Rinaldi, V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part III – impact ionization", *IEEE Trans. Electron Devices*, vol. 53, pp. 1683-1697, July 2006

Figure captions:

1. 3-D plot of the characteristics of an HBT in the I_c - V_{ce} - V_{be} space. The ridge of the mountain like surface is the SOA boundary.
2. 3-D SOA curve and its projections on the V_{be} - V_{ce} , I_c - V_{ce} , V_{be} - I_c planes.
3. Device I-V characteristics with various V_{be} inputs. The bend-over points are the places that the device becomes unstable. So the connection of the bend-over points is the SOA boundary.

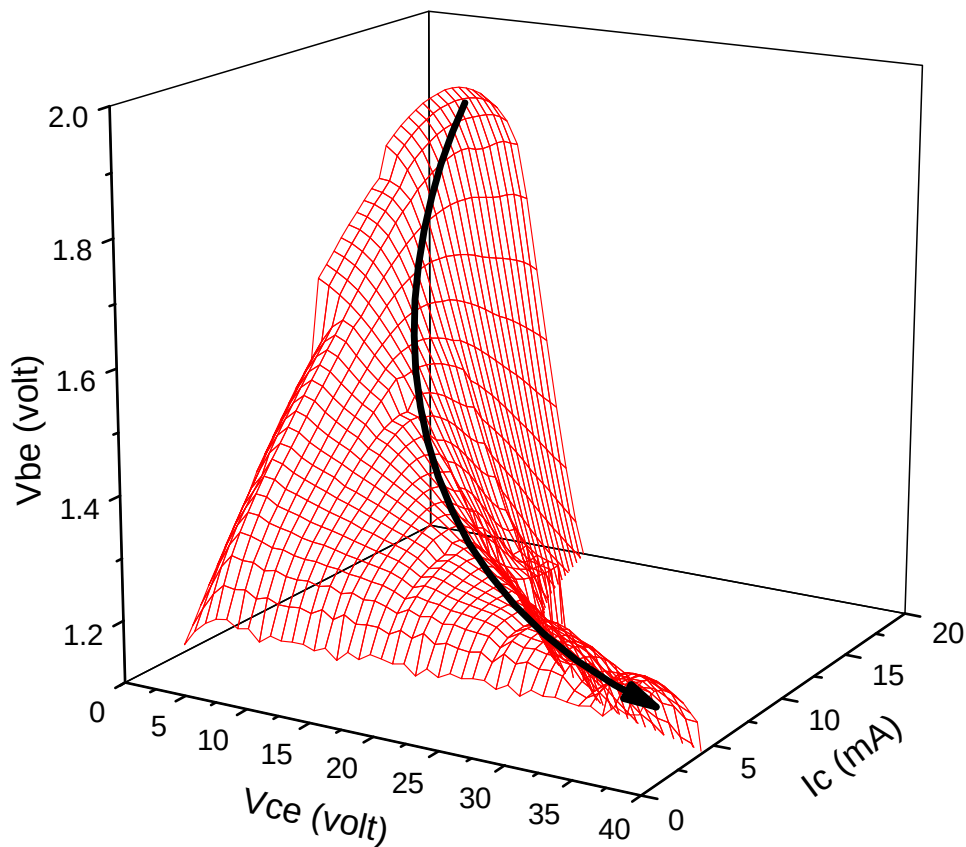


Fig. 1

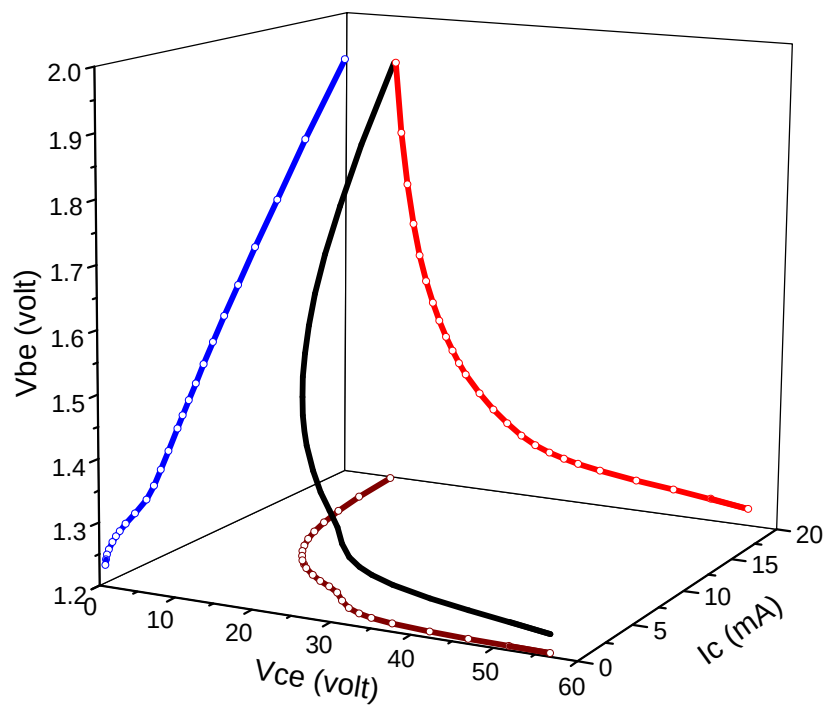


Fig. 2

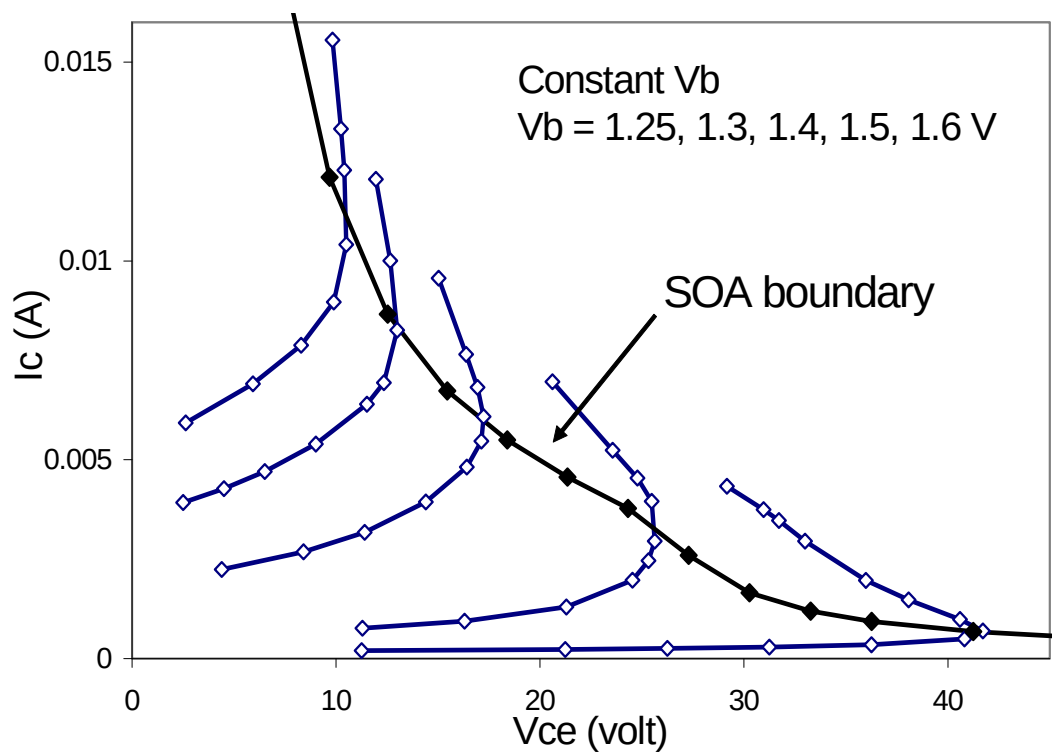


Fig. 3

行政院國家科學委員會補助專題研究計畫 ☐ 成果報告
☒ 期中進度報告

基地台所需之高崩潰電壓異質介面電晶體研究(1/2)

計畫類別：☒ 個別型計畫 ☐ 整合型計畫

計畫編號：NSC 94-2215-E-009-060-

執行期間：94 年 8 月 1 日至 95 年 7 月 31 日

計畫主持人：李建平

共同主持人：

計畫參與人員：廖志豪、李建騏

成果報告類型(依經費核定清單規定繳交)：☒ 精簡報告 ☐ 完整報告

本成果報告包括以下應繳交之附件：

☐ 赴國外出差或研習心得報告一份

☐ 赴大陸地區出差或研習心得報告一份

☐ 出席國際學術會議心得報告及發表之論文各一份

☐ 國際合作研究計畫國外研究報告書一份

處理方式：除產學合作研究計畫、提升產業技術及人才培育研究計畫、列管計畫及下列情形者外，得立即公開查詢

☐ 涉及專利或其他智慧財產權，☐ 一年☐ 二年後可公開查詢

執行單位：國立交通大學電子工程學系

中 華 民 國 95 年 5 月 31 日