

行政院國家科學委員會專題研究計畫 期中進度報告

碳管與電極接觸阻抗、蕭基接面、多閘極元件、高頻特性、 記憶單元應用之研究

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Chinese Abstract

本計畫為奈米國家型科技計畫「單層奈米碳管前瞻奈米電子與光電元件之組裝、製程及元件特性研究」之第二子計畫「碳管與電極接觸阻抗、蕭基接面、多閘極元件、高頻特性、記憶單元應用之研究」第一年度。計畫重點包括金屬與奈米碳管接觸阻抗、奈米碳管記憶元件、奈米碳管電晶體高頻特性等三個部份。接觸阻抗部分，根據氧氣吸附碳管對電子能量的影響，確認金屬與吸附於碳管之氧形成介面金屬氧化物是影響接觸阻抗之主要因素。記憶元件部分，確認利用遲滯現象作為記憶元件，其切換速度約 400 μ sec，回復時間約 1000sec。高頻特性分析部分，已完成測試結構設計以及光罩製作，元件製作尚在進行中。

關鍵詞：奈米碳管、奈米碳管電晶體、接觸阻抗、遲滯現象、記憶元件、射頻特性

English Abstract

This is the second task of the National Project “In-situ Assembly of Novel SWNT-based Electronic and Opto-electronic Devices”. The task title is “Process and characterization technologies for novel field effect transistors”. The topics in the first year include contact resistance between metal and CNT, CNT memory device, and high frequency characterization of CNTFET. In the part of contact resistance, we provide strong experimental evidence to prove that the contact resistance is closely related to the oxygen adsorption on CNT. For the memory application, the switching speed and retention time of CNTFET are extracted, for the first time, to be 400 μ sec and 1000sec, respectively. A mask set for the RF characterization of CNTFETs has been designed. Devices for RF characterization are under processing.

Keywords: carbon nanotube, carbon nanotube transistor, contact resistance, hysteresis phenomenon, memory device, RF characteristics.

Introduction

It has been reported that a semiconducting SWNT lying across two metallic electrodes, with a proper gate voltage control, could exhibit switching

behavior analogous to a p-channel field effect transistor (FET) in air and n-channel FET after being annealed in vacuum [1, 2]. According to the 2003 ITRS roadmap, the driving current density is to exceed 2.4 mA/ μ m by 2016. To reach this target, it relies on the continuous scale down of channel length and gate dielectric thickness. Novel techniques to improve carrier mobilities are also required. The development of high mobility SiGe, high-k dielectrics/metal gate and low-k interconnect for devices beyond 45 nm critical dimension have been aggressively developed in the traditional semiconductor industry. Meanwhile, several high performance CNT-FETs with equivalent driving current density as high as 3.75 mA/ μ m have been reported [3]. New records have also been achieved, such as mobility higher than 3000 cm²/V-sec [4], transconductance higher than 0.65 times that of the quantum conductance [5], subthreshold swing lower than 80 mV/decade [3], and I_{on}/I_{off} ratio higher than 10⁶ [6]. Recently, a 5-stage ring oscillator has been reported recently. The frequency is higher than 50 MHz [7]. All of these indicate that CNT-FET is a promising alternative than Si MOSFET, to stay on course in the ultimate ITRS roadmap.

Since the original CNTFET is a Schottky barrier device, the current flow is controlled by the Schottky barrier between metal and CNT at source/drain contacts. Ambipolar characteristic and poor driving capability are the major drawbacks of Schottky barrier devices. Those published high-performance CNTFETs used chemically or electrostatically doped S/D extension and S/D ohmic contact to achieve better performance. Therefore, low contact resistance between metal and CNT is required to fabricate high performance CNT transistors and low resistance interconnects. Therefore, in this sub-task, we will focus on the metal/CNT contact properties, high performance CNTFET devices, as well as the RF characterization of CNTFET.

Objective

Various metals and metal alloys including Pt-based alloys, Pd-based alloys, etc. with various work functions will be

developed to produce desirable contact characteristics with good thermal stability and adhesion. Metal systems to produce low and stable contact resistance will be developed. The impact of pre-metal deposition and post-metal deposition treatments on contact resistance will be investigated. Metal/CNT Schottky contact will be fabricated. The effective Schottky barrier height will be extracted.

The hysteresis phenomenon of I_{ds} - V_{gs} curve of CNT FET has been reported in literature [8-11]. This phenomenon reveals the possibility of memory application. In this sub-task, we will try to clarify the mechanism. The process effect on the hysteresis will be studied. The stability and repeatability will be controlled. Write-speed, read-speed, erase-speed, signal retention time, and endurance will be comprehensively characterized.

It has been proposed in literature that the CNT-FET can operate at very high frequency. The cut-off frequency is expected to be higher than 10 THz [12]. However, RF characteristics of CNT-FET have not been reported yet [13]. The limited experiments using back-gate structure and the overlap between gate to source/drain pad appeared to degrade the device performance. In this sub-task, the team members will design top gate CNT-FET for RF characterization. S-parameters up to 50 GHz will be measured using network analyzer system. Device structure optimization for RF operation as well as device modeling will be investigated.

Experiments

A four-terminal metal-on-CNT structure was used to extract the contact resistance between metal and CNT. CNTs were dispersed on oxidized Si wafers. E-beam lithography and metal lift-off processes were employed to define metal patterns. The successful test structures were identified by SEM inspection. The schematic test structure and the R_c extraction procedure are shown in Fig.1. Post-metal annealing (PMA) was performed

to evaluate the effect of thermal annealing.

The multi-terminal contact structures fabricated in the sub-task (1) are used as back-gated CNTFETs in this sub-task. Any test structures with two metal/CNT contacts could be used. Either SiO_2 or Si_3N_4 was used as gate dielectric. Hysteresis effect was measured under various environments to clarify the mechanism. The write/erase speed was studied using the apparatus set up as shown in Fig.2.

To fabricate nanotube transistors, we start with a degenerately Boron doped silicon wafer. Next, a $1.3\mu\text{m}$ thick SiO_2 was thermally grown in a PECVD system as shown in Fig.3(a). Next, substrate contact holes were patterned by electron beam lithography (EBL) and wet etching processes as shown in Fig.3(b). CNTs produced by laser ablation method were dispersed from a Dimethyl formamide(DMF) solution by spinning onto the substrate as shown in Fig.3(c1). Next, Source and Drain pads were patterned on the substrate by EBL. Source/Drain contact metal was sputtering deposited at a base pressure of 10^{-6} Torr followed by a standard lift-off process as shown in Fig.3(d). The spacing between Source/Drain is varied. The length of CNTs between contact pads ranges from 0.2 to $0.5\mu\text{m}$. Next, a 20 nm thick oxide or nitride gate dielectric was deposited by a PECVD system at 300°C . The contact holes for source/drain contact were patterned by EBL and wet etching processes as shown in Fig.3(e). Top gate was further patterned by EBL and metal lift-off processes again as shown in Fig.3(f). For comparison, CNTs grown by a CVD system were also fabricated as shown in Fig.3(c2). The catalytic pads were patterned by deep UV lithography and lift-off processes.

Results and Discussion

Fig.4(a) and (b) show the correlation between contact resistance (R_c) and the work function of metal and the heat-of-formation of metal oxides, respectively. It is interesting that Pt and CNTs has the largest work function

difference but shows the lowest contact resistance. The work function difference between Al and CNTs is small, but the contact resistance is higher than 10G ohm. In fact the Al/CNT contact is almost open. On the other hand, the contact resistance is better correlated with the heat-of-formation of metal oxides. The lower heat-of-formation of metal oxide shows lower contact resistance except Cu. These results have been obtained in last year. The electronic structure of metal-CNTs contact with or without oxygen adsorption has been calculated by Dr. Park and Dr. Hong in 2005 [14]. Upon oxygen adsorption, the tunneling barrier increases due to oxidation. The transmission probability for CNT/O/Al structure is 85% lower than that for CNT/Al structure. The contamination of one oxygen monolayer could result in one order of magnitude higher contact resistance. We assume that the metals with high heat-of-formation of metal oxide react with the oxygen adsorbed on CNTs to form a metal oxide interfacial layer. Because Al-oxide and Ti-oxide are good insulators, the contact resistances are very high. Cu is easily to be oxidized, therefore, although the heat-of-formation of Cu is low, the contact resistance is still very high.

Fig.5 shows the typical hysteresis phenomenon of a back-gated CNTEFT in ambient. By increasing humidity, increasing polar molecules adsorption, increasing voltage sweep rate, the hysteresis loop is enlarged. By capping a PECVD SiO₂ layer, capping a PMMA layer, measuring in vacuum, the hysteresis loop is almost diminished at low voltage. However, increasing the range of voltage sweep, hysteresis phenomenon still exists. These experiments imply that the both the polar molecule adsorption and carrier injection play role on the hysteresis phenomenon.

Fig.6 shows the write waveform and the erase wave form of the CNTFET. The switching speed is about 400μsec. Fig.7 shows the retention characteristics of the CNTFET under various gate biases. The retention time is in the order of 1000 sec and

the drain current is unstable as the gate is floating. Table 2 compares the basic parameters of various memory devices.

For the RF characterization, in the past 9 months, we finished literature survey, test structures design, and mask set fabrication. Test devices are still under processing. The test structure is shown in Fig.8 and the floor plan is shown in Fig.9. The metal pad is designed for G-S-G RF probing. The substrate is connected to source via the substrate contact hole to minimize the noise. Devices with different gate length and different S/D metal distance were designed. Devices have been processed to the step of gate dielectric patterning.

Summary and Conclusions

In these months, we have the following achievements :

- (1) Find out a physical basis to explain the correlation between contact resistance of the heat-of-formation of metal oxide. To obtain ideal ohmic contact between metal and CNT, low work function difference and clean interface are pre-requisitions.
- (2) Both polar molecule adsorption and carrier injection play role on the hysteresis effect of CNTFET. Stable CNT memory device is expected if the molecule adsorption could be avoided. The write/erase speed is higher than Flash memory and the retention time is longer than DRAM/SRAM. The CNT memory might be used in some special circumstances.
- (3) RF CNTFET test structures have been designed. The test devices are under processing. The infra-structure for RF characterization of CNTFET is ready.

Self-evaluation

In the past several months, we followed the plan scheduled in proposal. The progress is well controlled. Several important results have been achieved and been summarized in previous section.

The research assistances gather plenty experiences on the basic property analysis of CNT, process technology of CNTFET fabrication, and electrical characterization

of CNTFET. These trainings provide a solid basis for the future investigation of high performance CNTFETs.

Part of the results of this project has been published in the international conference of VLSI-TSA [15].

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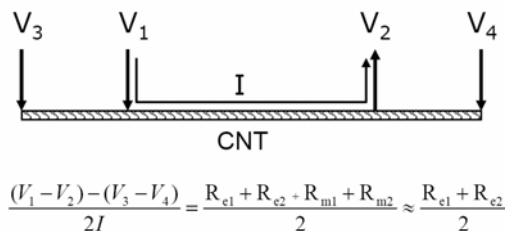


Fig.1 Schematic test structure and the R_c extraction procedure.

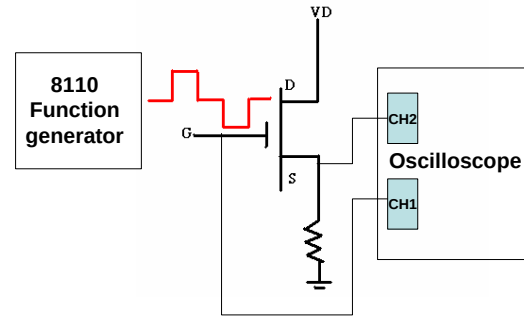


Fig.2 Apparatus set up for write/erase speed evaluation of a CNT memory device.

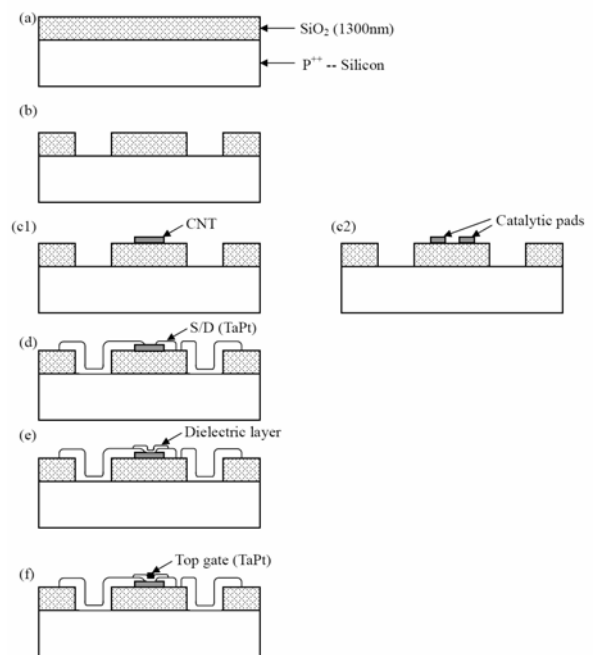


Fig.3 Process flow of the CNTFETs for RF characterization.

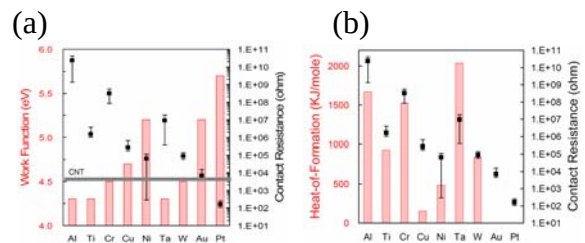


Fig.4 Correlation between contact resistance and (a) work function of metal and (b) heat-of-formation of metal oxides.

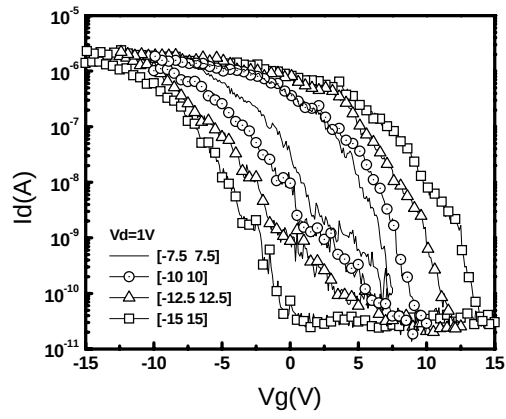


Fig.5 Typical hysteresis phenomenon of a back-gated CNTEFT in ambient.

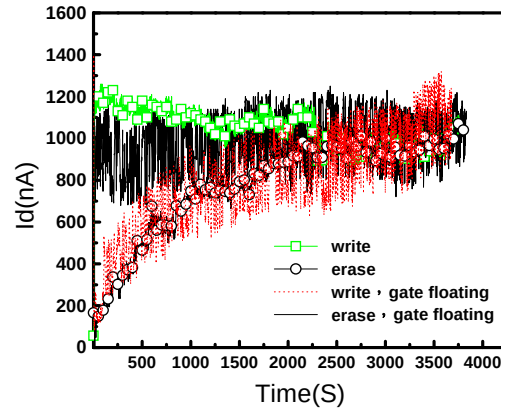


Fig.7 Retention characteristic of the CNT memory device under various gate biases.

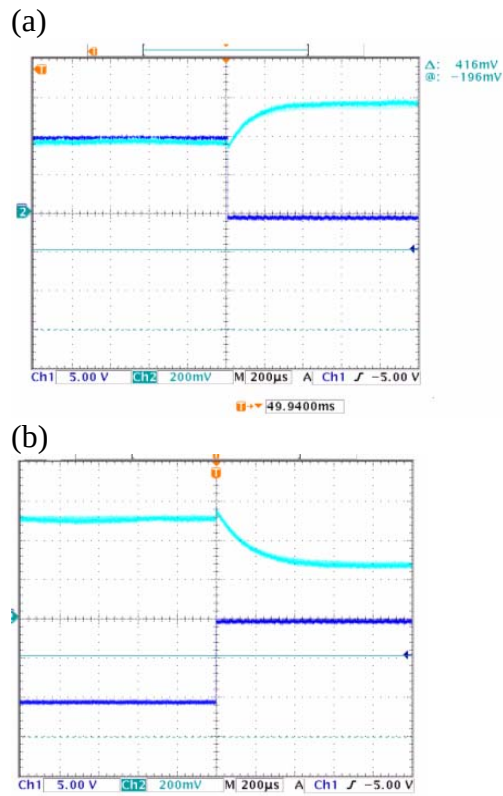


Fig.6 (a) Write waveform and (b) erase wave form of the CNT memory device. The switching speed is about 400 μ sec.

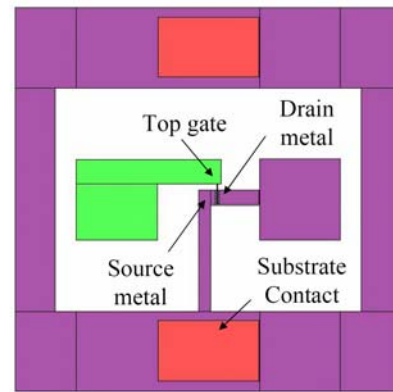


Fig.8 Test structure for RF characterization of CNTFET.

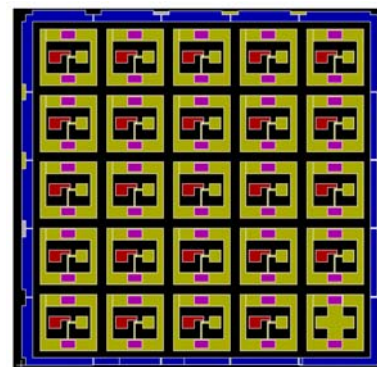


Fig.9 Floor plan of the test site.