

# A New Simplified Threshold-Voltage Model for n-MOSFET's with Nonuniformly Doped Substrate and Its Application to MOSFET's Miniaturization

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**Abstract**—The formulation, verification, and application of a new simplified 2-D threshold voltage model for n-MOSFET's with nonuniformly doped substrate profile are provided, in which the averaged normal field at the Si/SiO<sub>2</sub> interface in the active channel is quoted from a simplified solution of two-dimensional Poisson equation using the Green function technique. Starting with the expression of this average normal field, a simple threshold-voltage model for short-channel n-MOSFET's with nonuniformly doped substrate profile is explicitly expressed in terms of device structures and terminal voltages by considering parabolic source-drain boundary potentials. Moreover, the effects of the junction depth on the threshold voltage are examined in detail. It is shown that the DIBL effect cannot be completely eliminated by simply increasing the substrate doping concentration. Comparisons among developed model, 2-D numerical analysis, and experimental data have been made and the accuracy of the developed analytical model has been verified. In addition, a direct extension of our model to the case of uniformly doped substrates leads to a new constraint equation for device miniaturization.

## NOMENCLATURE

|                      |                                                                                                        |
|----------------------|--------------------------------------------------------------------------------------------------------|
| $\bar{E}_s$          | The averaged normal field at the Si/SiO <sub>2</sub> interface in the active channel.                  |
| $I_{DS}$             | The drain current.                                                                                     |
| $k$                  | ( $\equiv  dV_{TH}/dV_{DS} $ ) the drain-induced barrier lowering (DIBL) factor.                       |
| $L$                  | The effective channel length.                                                                          |
| $L_{min}$            | The minimum channel length above which the long-channel characteristics can be maintained.             |
| $N_A(y)$             | The superposed nonuniform doping distribution in the substrate.                                        |
| $N_{AB}$             | The base doping concentration in the substrate.                                                        |
| $N_S^*(y)(N_B^*(y))$ | The effective substrate doping distribution viewed from the Si/SiO <sub>2</sub> interface (substrate). |
| $q$                  | The electronic charge ( $= 1.6 \times 10^{-19}$ Coul).                                                 |
| $R_j$                | The source/drain junction depth.                                                                       |

|                             |                                                                                           |
|-----------------------------|-------------------------------------------------------------------------------------------|
| $T_{ox}(C_{ox})$            | The thickness (capacitance per unit area) of the gate oxide.                              |
| $V_{BI}$                    | The built-in potential between the source and the channel.                                |
| $V_{BS}, V_{GS}, V_{DS}$    | The substrate-, gate-, and drain-to-source bias voltages, respectively.                   |
| $V_{TH}$                    | The threshold voltage.                                                                    |
| $W$                         | The channel width.                                                                        |
| $y_d$                       | The depletion width in the channel region.                                                |
| $y_{do}$                    | The depletion width in the channel region without considering any two-dimensional effect. |
| $y_{JS}(y_{JD})$            | The vertical depth of the depletion region at the source (drain) end.                     |
| $\epsilon_s(\epsilon_{ox})$ | The dielectric permittivity of silicon (oxide).                                           |
| $\phi_{sinv}$               | The surface potential at the onset of strong inversion.                                   |
| $\phi_{y_d}$                | The built-in potential at the bottom of the depletion region.                             |
| $\bar{\Psi}(x, 0)$          | The weighted surface potential.                                                           |
| $\bar{\Psi}(x, y_d)$        | The weighted boundary potential at the bottom of the depletion region.                    |
| $\Psi_S(y) (\Psi_D(y))$     | The boundary potential at the source (drain) end.                                         |

## I. INTRODUCTION

THE threshold voltage of MOSFET's, which has always been the major concern of device scaling, is closely related to device structure parameters (e.g., oxide thickness, junction depth, gate length, etc.) and terminal voltages. The increasing complexity of modern MOS device structure requires clear understanding on the behavior of threshold voltage, and many efforts have been devoted to the investigation of this electrical parameter.

Conventional long-channel theories were first challenged by the introduction of channel implantation in modern MOS devices [1]. Another challenge comes from the existence of source/drain diffusion islands. To physically interpret the short-channel effect, the roles of source/drain islands were first emphasized in the simplified Yau's *charge-sharing scheme* [2] for the threshold-voltage model with uniform substrate doping profile. The charge-sharing scheme had been improved by many authors (e.g., [3] and [4]), and the channel-length depen-

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dence of threshold voltage could be simulated with acceptable deviation. This scheme helps us understand the behavior of short-channel MOSFET devices, however its mathematical treatment with the addition of artificial charge partition is too rough to reveal any further physical insight of devices. As device dimensions fall into submicrometer range, the charge-sharing scheme fails to overcome these drawbacks.

Besides the charge-sharing scheme, another strategy to attack the above problems is to directly solve the two-dimensional Poisson equation analytically [5]–[13]. Recently, a simplified threshold-voltage model for surface-channel MOSFET's with nonuniform substrate doping profile has been proposed by Lin and Wu [13], which is based on solving the *depletion-approximated* two-dimensional Poisson equation using the Green function solution technique. The effects due to short channel, depletion-width broadening (increase of substrate depletion width with the two-dimensional effects), and charge screening (insensitivity of threshold voltage to substrate bias for short-channel devices) can be described by this model. The expression for the average normal field at the oxide/semiconductor interface obtained in [13] will be utilized to derive an explicit form for the threshold voltage of n-MOSFET's in this paper. The resulting equations for the threshold voltage are mainly composed of structure parameters and terminal voltages. To compensate the errors caused by the assumptions made on the boundary potentials, a parametric approach is adopted and the behavior of the drain-induced barrier lowering (DIBL) effect [14] is analyzed in detail simultaneously.

The major problem in device scaling is to explore the shrinkage law for device. The constant-field strategy [15], [16] was proposed to scale the physical dimensions and potentials of MOSFET's with uniformly doped substrate, while keeping the field pattern in the scaled devices unchanged. One [15] or two [16] scaling factors were introduced to cover the scaling of all the parameters. Basically, the constant-field scaling strategy plays some roles as the device operation is governed by the electric field. As this is not the case, this strategy contributes nearly nothing to miniaturization consideration. Based on detailed observation from the subthreshold behavior of MOSFET's, Brews *et al.* [17] proposed an empirical law which serves as a constraint on the relations of device structures to guarantee the long-channel characteristics for scaled devices. Recently, an improved miniaturization guide was proposed by Ng *et al.* [18]. In this paper, we'll extend our model to the case of uniformly doped substrates. Under some assumptions, a constraint relation similar to those developed by Brews *et al.* and Ng *et al.* can be derived.

## II. MODEL FORMULATION AND DISCUSSIONS

The cross-section view of a conventional n-MOSFET is shown in Fig. 1, in which the dashed curve indicates the edge of the depletion region in the substrate. With the aids of Green function solution technique, the two-dimensional Poisson equation in this rectangular domain was solved and the derived potential distribution can be expressed in terms of an infinite series of sine functions along the channel direction

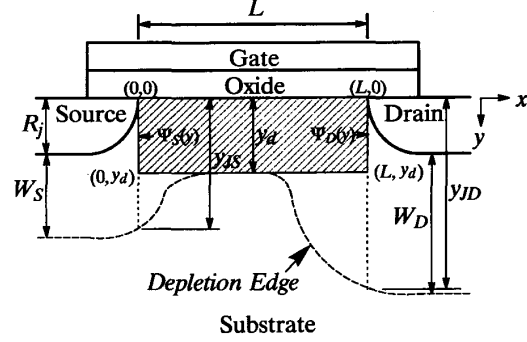


Fig. 1. The cross-section view of a conventional n-MOSFET. The shaded rectangular box is the analytic solution domain of the two-dimensional Poisson equation.

(i.e.,  $x$ -axis in Fig. 1) [13]. By differentiating the above two-dimensional potential distribution with respect to  $y$  at  $y = 0$ , we can compute the normal electric field at the Si/SiO<sub>2</sub> interface  $E_S(x)$ . Further simplification was made by averaging the field pattern  $E_S(x)$  by the corresponding eigenfunction. Consequently, the averaged surface normal field  $\bar{E}_S$  is

$$\bar{E}_S = \frac{q}{\epsilon_S} \int_0^{y_d} N_S^*(y) \frac{\sinh k_1(y_d - y)}{\sinh k_1 y_d} dy + \frac{q}{\epsilon_S} \int_0^{y_d} N_B^*(y) \frac{\sinh k_1 y}{\sinh k_1 y_d} dy \quad (1)$$

with  $k_1 \equiv \pi/L$ . The average normal field at the depletion edge has been neglected in (1).  $N_S^*(y)$  and  $N_B^*(y)$  are the effective doping distributions viewed from the interface and the bottom of the depletion edge in the channel region, respectively, and are written as

$$N_S^*(y) = N_A(y) - \frac{\epsilon_S}{2q} \left( \frac{\pi}{L} \right)^2 [\Psi_S(y) + \Psi_D(y) - 2\bar{\Psi}(x, 0)] \quad (2a)$$

and

$$N_B^*(y) = N_A(y) - \frac{\epsilon_S}{2q} \left( \frac{\pi}{L} \right)^2 [\Psi_S(y) + \Psi_D(y) - 2\bar{\Psi}(x, y_d)]. \quad (2b)$$

Because of the existence of  $\Psi_S(y)$  and  $\Psi_D(y)$ , both  $N_S^*(y)$  and  $N_B^*(y)$  are less than the originally implanted profile,  $N_A(y)$ . The weighting function of  $N_S^*(y)$  in (1) (i.e.,  $\sinh k_1(y_d - y)/\sinh k_1 y_d$ ) indicates that the charge controllability of gate voltage decreases rapidly along the depth as  $y_d \gtrsim L$ , due to the exponential behavior of this weighting function. This effect is denoted as the "charge-screening" effect in [13]. Experimentally, the charge-screening effect is demonstrated by the weak substrate sensitivity of short-channel MOS devices. On the other hand, the second term on the RHS of (1) is related to the *depletion-width broadening* effect since  $y_d$  is determined by  $N_B^*(y)$ . Shorter channel length and/or larger drain voltage will result in further deviation of  $N_B^*(y)$  from  $N_A(y)$ . Since the surface potential depends on  $N_B^*(y)$ , a larger  $y_d$  is necessary to achieve the same surface potential as the two-dimensional effects are more pronounced.

For surface-channel devices, the threshold voltage  $V_{TH}$  can be simply expressed by

$$V_{TH} = V_{FB} + \overline{\Psi(x, 0)}_{inv} + \frac{\epsilon_S \bar{E}_S}{C_{ox}}. \quad (3)$$

Note that (3) is a direct result of Gauss law. Equations (1) and (2) are then substituted into (3) for threshold computation. The boundary potentials used for the shaded rectangle in Fig. 1 are

$$\Psi_{Sm}(y) = (V_{BI} - V_{BS}) \left(1 - \frac{y}{y_{JS}}\right)^2 + V_{BS} \quad \text{for } 0 \leq y \leq y_{JS} \quad (4a)$$

$$\Psi_{Dm}(y) = (V_{BI} + V_{DS} - V_{BS}) \left(1 - \frac{y}{y_{JD}}\right)^2 + V_{BS} \quad \text{for } 0 \leq y \leq y_{JD} \quad (4b)$$

where the parabolic source/drain boundary potentials are used and the two average potentials are expressed by

$$\overline{\Psi(x, 0)}_{inv, m} = \phi_{sinv} \quad (4c)$$

and

$$\overline{\Psi(x, y_d)}_m = \phi_{yd} + V_{BS}. \quad (4d)$$

Note that the subscript  $m$  means that these terms are assumed in our model. Observation from 2-D numerical analysis, it shows that the parabolic potentials,  $\Psi_{Sm}(y)$  and  $\Psi_{Dm}(y)$ , are good enough as long as the drain voltage  $V_{DS}$  is small. As  $V_{DS}$  is large, the “field-retrograde” effect [11] will occur. To take this effect into consideration, a piece-wise parabolic boundary potential at the drain side can be assigned [11], [12]. However, a careful inspection on (1) and (2) shows that the detail form of  $\Psi_D(y)$  is not the major concern, but is its integration. For simplicity, we adopt the parabolic potentials for  $\Psi_{Sm}(y)$  and  $\Psi_{Dm}(y)$ . The error due to the ignorance of the field retrograde effect can be corrected by other considerations as will be discussed later.

Combination of (1)~(4) gives

$$V_{TH} = V_{FB} + \phi_{sinv} + \frac{Q_{Beff}}{C_{ox}} - \Delta V_{TH} + L.T. \quad (5)$$

where

$$\begin{aligned} Q_{Beff} &= q \int_0^{y_d} N_A(y) \frac{\sinh k_1(y_d - y) + \sinh k_1 y}{\sinh k_1 y_d} dy \\ &= q \int_0^{y_d} N_A(y) G(y) dy \end{aligned} \quad (6)$$

is the effective depletion charge density per unit area controlled by the gate;  $\Delta V_{TH}$  is the effective reduction of the threshold voltage due to the two-dimensional effects and is written as

$$\begin{aligned} \Delta V_{TH} &= \pi \frac{\epsilon_S}{\epsilon_{ox}} \frac{T_{ox}}{L} \frac{\cosh k_1 y_d - 1}{\sinh k_1 y_d} \\ &\quad \times [\beta_S V_{BI} + \beta_D (V_{BI} + V_{DS}) \\ &\quad - (\beta_S + \beta_D - 1) V_{BS} - \phi_{sinv}] \end{aligned} \quad (7)$$

where  $\beta_S$  and  $\beta_D$  are the integration results of the parabolic terms of  $\Psi_{Sm}(y)$  and  $\Psi_{Dm}(y)$ , respectively, i.e.,

$$\beta_S = k_1 \sinh k_1 y_d \int_0^{y_d} \left(1 - \frac{y}{y_{JS}}\right)^2 G(y) dy \quad (8a)$$

and

$$\beta_D = k_1 \sinh k_1 y_d \int_0^{y_d} \left(1 - \frac{y}{y_{JD}}\right)^2 G(y) dy. \quad (8b)$$

The final term of (5) sums up all of the deviations resulting from the approximations made on the boundary potentials.  $L.T.$  is the abbreviation of “Lost Terms” and consists of four components:

$$\begin{aligned} L.T. &= \frac{1}{2} \frac{\epsilon_S}{C_{ox}} \left(\frac{\pi}{L}\right)^2 \int_0^{y_d} [\Psi_{Sm}(y) - \Psi_S(y)] G(y) dy \\ &\quad + \frac{1}{2} \frac{\epsilon_S}{C_{ox}} \left(\frac{\pi}{L}\right)^2 \int_0^{y_d} [\Psi_{Dm}(y) - \Psi_D(y)] G(y) dy \\ &\quad + \left[ \frac{\epsilon_S}{C_{ox}} \frac{\pi \cosh k_1 y_d - 1}{L \sinh k_1 y_d} + 1 \right] \\ &\quad \times (\overline{\Psi(x, 0)}_{inv} - \phi_{sinv}) \\ &\quad + \left[ \frac{\epsilon_S}{C_{ox}} \frac{\pi \cosh k_1 y_d - 1}{L \sinh k_1 y_d} + 1 \right] \\ &\quad \times [\overline{\Psi(x, y_d)} - (\phi_{yd} + V_{BS})]. \end{aligned} \quad (9)$$

Obviously, the RHS of (9) includes the deviations of the boundary potentials from source, drain, surface, and the bottom boundaries in sequence. The parabolic potential  $\Psi_{Sm}(y)$  will not cause significant error since the source is generally grounded. Besides, the deeper charges in the substrate hardly affect the potential at the surface. Therefore, the last term in (9) can be neglected. Consequently,  $L.T.$  is mainly contributed by the inaccuracy of drain and surface boundary potentials. It can be understood that the term  $(\overline{\Psi(x, 0)}_{inv} - \phi_{sinv})$  produces a shift of the threshold voltage and is nearly independent of the external voltages. Further simplification can be made by noting the relation between (8b) and the term  $(\Psi_{Dm}(y) - \Psi_D(y))$ . We have discussed that the field retrograde effect can be described by a piece-wise parabolic potential for  $\Psi_D(y)$ . The term  $(\Psi_{Dm}(y) - \Psi_D(y))$  is also parabolic under this consideration. Equation (8b) can then be used to replace the second term on the RHS of (9). A fitting parameter  $a$  is introduced to compensate the integration deviation. As a consequence,  $L.T.$  is eventually approximated by

$$L.T. \simeq \frac{\pi}{2} \frac{\epsilon_S}{\epsilon_{ox}} \left(\frac{T_{ox}}{L}\right) \frac{\beta_D (1 - a)}{\sinh k_1 y_d} V_{DS} \quad (10)$$

where the behavior of  $a$  requires conscientious investigation. To eliminate the uncertainty of channel profile, we compare the above equations with the threshold voltages extracted from numerical simulation data. The simulator used here is a conventional 2-D drift-diffusion MOS simulator-SUMMOS (SubMicron MOSFET) [19]. To simulate the implanted profile, the SUMMOS uses the Gaussian functions:

$$N_A(y) = \sum_i \frac{\Phi_i}{\sqrt{2\pi} \Delta R_{pi}} \exp \left[ -\frac{(y - T_{ox} + R_{pi})^2}{2\Delta R_{pi}^2} \right] + N_{AB} \quad (11)$$

where  $\Phi_i$ ,  $R_{pi}$ , and  $\Delta R_{pi}$  are the dose, range, and straggling of the  $i$ -th implantation, respectively. Table I lists the structure parameters used to evaluate our model. For convenience, the device described in Table I is called Device A and the cylindrical junction curvature is assumed. To speed up the

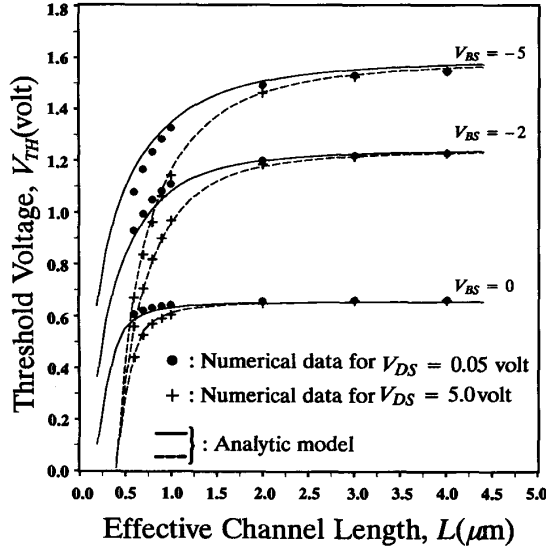


Fig. 2. Comparison between the results of our analytic model (— and —) and the threshold voltages extracted from numerical simulation (● and +). The device structure and parameters used for simulation are described in Table I.

TABLE I  
THE STRUCTURE PARAMETERS OF DEVICES SIMULATED BY SUMMOS. THE PARAMETERS OF THE EQUIVALENT STEP PROFILES ARE ALSO LISTED. THIS DEVICE IS CALLED DEVICE A

|                              |                       |
|------------------------------|-----------------------|
| $T_{ox}(\text{\AA})$         | 250                   |
| $V_{FB}(\text{volt})$        | -1.0                  |
| $N_{AB}(\text{cm}^{-3})$     | $8.00 \times 10^{15}$ |
| $\Phi(\text{cm}^{-2})$       | $1.00 \times 10^{12}$ |
| $\Delta R_{p1}(\mu\text{m})$ | 0.07                  |
| $R_{p1}(\mu\text{m})$        | 0.1                   |
| $N_{AS1}(\text{cm}^{-3})$    | $4.67 \times 10^{16}$ |
| $Y_{AS1}(\mu\text{m})$       | 0.184                 |

computation efficiency, the Gaussian profile is transformed into the equivalent step one and the lower part of Table I shows the corresponding parameters. The filled circles and the plus signs shown in Fig. 2 are the  $V_{TH}$ 's determined from the numerical  $I-V$  data by the method described in [13].

The magnitude of  $a$  is then extracted by comparing our model with the numerical  $V_{TH}$ 's. Fig. 3 illustrates the variation tendency of  $a$  with the ratio  $R_j/L$  extracted from the data points in Fig. 2 and several physical features are revealed. It is noted that the source/drain islands are excluded from the shaded rectangle in Fig. 1. Special considerations are necessary to incorporate the effect of  $R_j$  into the analytic model. Previous discussions on the boundary potentials imply that the ambiguities of  $\Psi_{Sm}(y)$  and  $\Psi_{Dm}(y)$  will blur the

effect of  $R_j$  on  $V_{TH}$ . It must be precisely corrected by the behavior of  $a$ . In Fig. 3, the slightly random distribution of  $a$ 's values in the range of small  $R_j/L$  is due to the negligible threshold reduction. For devices with long channel and/or shallow S/D junction depth (i.e.,  $R_j/L$  is small), the effect of  $V_{DS}$  on  $V_{TH}$  is small and hence  $a$  is more sensitive to the soft fluctuations occurred in  $V_{TH}$  determination. At some fixed  $V_{BS}$ ,  $a$  tends to saturate as  $R_j/L$  is large. It tells us that the strength of the short-channel effect will not expand infinitely with  $R_j$ . As  $R_j$  is deep enough, the loss of flux due to further increase of  $R_j$  will not be experienced by gate, because those charges additionally terminated by the source/drain islands are deep in the substrate and have nearly no contribution to the surface potential. Furthermore, when the DIBL effect is significant,  $a$  increases with  $|V_{BS}|$ . More definitely,  $a$  is enlarged by the extension of  $y_d$ . Careful examination on Fig. 2 indicates that the channel length below which the  $V_{TH}$  begins to decline remarkably increases with  $|V_{BS}|$ . According to the interpretation of the charge-sharing scheme [2], the relative gate flux loss will increase with the boundary ratio of the shaded rectangle in Fig. 1 (i.e.,  $y_d/L$ ). The increase of  $a$  with  $y_d$  also recommends that the term  $L.T.$  is dominated by the second term on the RHS of (9). It has been reported that the depth of the region with the field retrograde effect, which is denoted by  $y_I$ , is nearly independent of  $V_{BS}$  [12], [13]. The physical reason is attributed to the charge screening effect [13]. As  $y \geq y_I$ , the deviation term  $(\Psi_{Dm}(y) - \Psi_D(y))$  is negligible. Roughly speaking, we have

$$\frac{\int_0^{y_d} [\Psi_{Dm}(y) - \Psi_D(y)] G(y) dy}{\int_0^{y_d} \Psi_D(y) G(y) dy} \approx \frac{\int_0^{y_I} [\Psi_{Dm}(y) - \Psi_D(y)] G(y) dy}{\int_0^{y_d} \Psi_D(y) G(y) dy}. \quad (12)$$

The increase of  $y_d$  and hence  $a$  reduces the deviation ratio and  $L.T.$  is reduced correspondingly.

The data points plotted in Fig. 3 are extracted from Device A with different  $R_j$ 's. It's interesting to note that the data points with different  $R_j$ 's under the same  $V_{BS}$  locate on a universal curve. It strongly implies that  $a$  is mainly related to  $R_j$ . An empirical equation can be used to fit the data points, which reads

$$a = a_0 \left( \frac{R_j}{L} \right)^n. \quad (13)$$

The solid curves in Fig. 3 are the results of (13). The power  $n$  represents the sensitivity of the DIBL effect to  $R_j$  and  $n = 0.80$  is used in Fig. 3. A similar power relation has been obtained by Ng *et al.* [18] with a value of 0.7, which is close to our result. The pre-factor  $a_0$  includes the  $V_{BS}$ -dependence of  $a$ . A good approximation is made by expressing  $a_0$  in terms of the one-dimensional depletion depth  $y_{do}$ . Besides, we note that a linear relation is sufficient to describe the behavior of  $a_0$ . Consequently,  $a_0$  is written as

$$a_0 = m y_{do} + a_{00}. \quad (14)$$

$a_{00} = 0.317$  and  $m = 0.785/\mu\text{m}$  are found. In (14),  $y_{do}$  is multiplied by  $m$  to improve the accuracy of our model

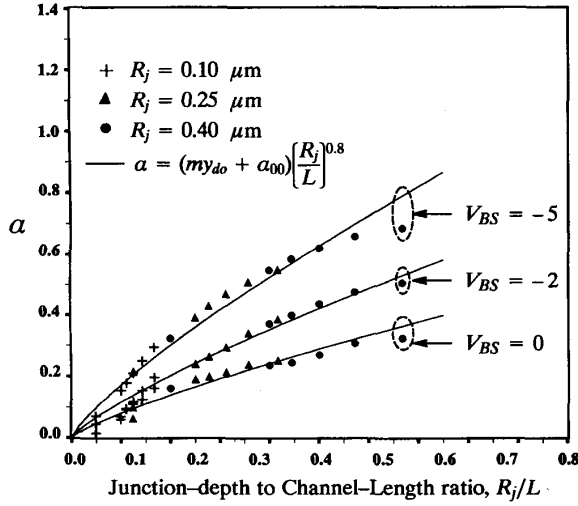


Fig. 3. The variations of the parameter  $a$  with the junction depth to channel length ratio ( $R_j/L$ ) for  $V_{BS} = 0, -2$  and  $-5$  volt. The data points (+,  $\bullet$ ,  $\blacktriangle$ ) are extracted from 2-D numerical analysis for Device A (see Table I) with different  $R_j$ 's. The solid curves are computed according to  $a = (my_{do} + a_{00}) \times (R_j/L)^n$  with  $m = 0.785/\mu\text{m}$ ,  $a_{00} = 0.317$ , and  $n = 0.80$ .

for simulating the enhanced charge-sharing effect caused by the "boundary-ratio variation" as mentioned previously. The nonvanishing  $a_{00}$  means that the DIBL effect cannot be completely eliminated by simply increasing the channel doping concentration. For convenience, we define the magnitude of the DIBL effect to be

$$k \equiv \left| \frac{dV_{TH}}{dV_{DS}} \right|. \quad (15)$$

To demonstrate the existence of the nonvanishing  $a_{00}$ , Fig. 4 shows the variation of the DIBL factor  $k$  extracted from numerical simulations (filled circles) with uniform substrate doping concentration  $N_{AB}$  for simplicity, in which  $R_j = 0.25 \mu\text{m}$  and  $L = 0.40 \mu\text{m}$  are used. The magnitude of  $k$  decreases with  $N_{AB}$  as expected, while it tends to level off as  $N_{AB}$  is high. Clearly, the finite value of  $k$  as  $N_{AB}$  is high is accounted for by the nonvanishing  $a_{00}$ . Therefore,  $a_{00}$  plays an important role as the device miniaturization issues are concerned. The physical picture revealed by  $a_{00}$  is the perpetual charge sharing by  $V_{DS}$ . Fig. 4 shows the result calculated by our model (solid curve) and the agreement is good. Note that a larger deviation in the low-doping region is observed due to the fact that the threshold reduction in this region is dominated by the punchthrough effect which is not considered in our model. Beyond this region, the deviation is small and this means that  $m$  and  $a_{00}$  are independent of the channel profiles.

Equations (10), (13), and (14) are then substituted into (5) to calculate the threshold voltage, and the solid and dashed curves in Fig. 2 are the calculation results. It is shown that our model agrees with the numerical data excellently and the error caused by the approximated boundary potentials is successfully corrected by the parameter  $a$ .

Our model can also be applied to LDD MOSFET's by simply replacing the heavily doped  $R_j$  by the lightly-doped  $R_j^-$ . Fig. 5 shows comparisons between the measured  $V_{TH}$ 's

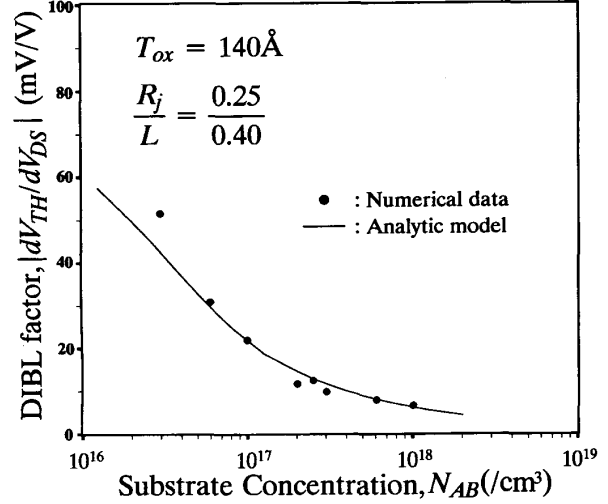


Fig. 4. The effect of uniform substrate doping concentration  $N_{AB}$  on the DIBL factor  $k$ .  $T_{ox} = 140 \text{ \AA}$ ,  $R_j = 0.25 \mu\text{m}$ , and  $L = 0.40 \mu\text{m}$  are used. The filled circles ( $\bullet$ ) are determined by 2-D numerical simulation. The solid curve (—) is calculated by our model.

and our model, in which the test devices are fabricated by the  $0.5\text{-}\mu\text{m}$  technology with the oxide thickness of  $110 \text{ \AA}$  and  $R_j^-$  of  $0.18 \mu\text{m}$ . Fig. 5(a) is the channel profile extracted from the threshold-voltage versus substrate-bias curve of a long-channel device by the nonlinear optimization algorithm in [21]. The effects of channel length and  $V_{DS}$  are shown in Fig. 5(b). Quite good agreements are obtained.

### III. APPLICATION TO MOSFET MINIATURIZATION

From the previous section, the accuracy of the developed threshold-voltage model has been verified by either numerical analyses or experimental data of short-channel n-MOSFET's. The miniaturization of n-MOSFET's based on the constraint of the drain-induced barrier lowering effect (e.g.,  $k \leq 20 \text{ mV/V}$ ) can be carried out by using our model through computer iteration. Due to the complicated coupling effects, a simple relation among the various structure parameters, which describes the shrinkage rule of each parameter after scaling, cannot be easily deduced from the complete model without further approximation. However, as the magnitude of the DIBL effect is small (e.g.,  $k \leq 20 \text{ mV/V}$ ), the charge-screening effect and the depletion-width broadening effect discussed in Section II can be neglected. Eventually, the depletion width  $y_d$  is not affected by any two-dimensional effect under our assumptions and can be replaced by  $y_{do}$ . The threshold-voltage model can be further simplified to be

$$V_{TH} = V_{FB} + \phi_{sinv} + \frac{Q_B(y_{do})}{C_{ox}} - \Delta V_{TH} \quad (16)$$

where  $Q_B(y_{do})$  is the depletion-charge density per unit area within  $y_{yo}$  and

$$\Delta V_{TH} = \frac{\pi^2 \epsilon_S}{2 \epsilon_{ox}} \frac{T_{ox}}{L} \frac{y_{do}}{L} [f_S V_{BI} + f_D (V_{BI} + a V_{DS}) - (f_S + f_D) V_{BS}]. \quad (17)$$

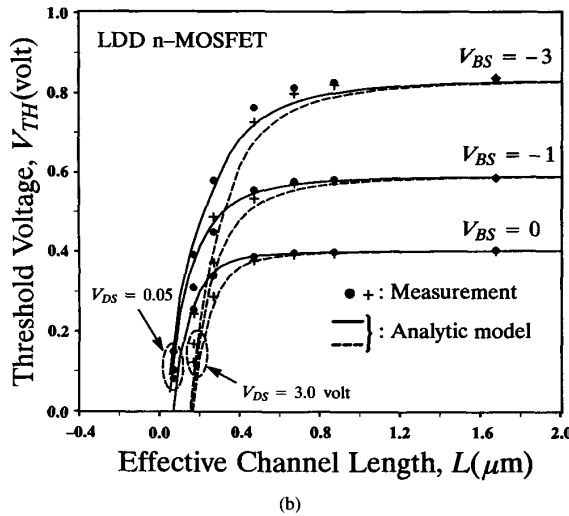
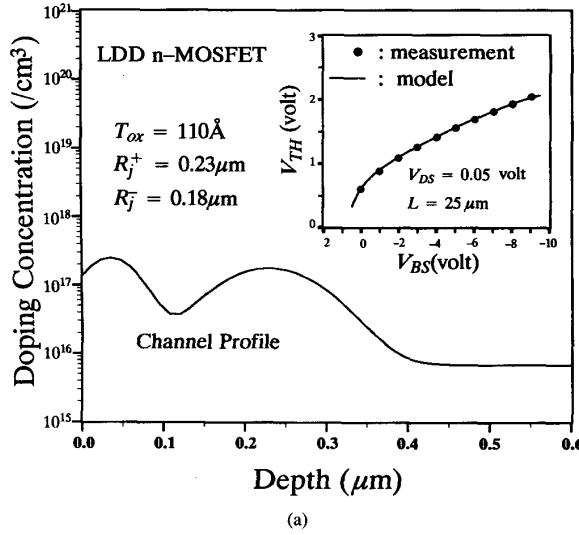


Fig. 5. Application of the developed analytic model to the calculation of the threshold voltages of LDD MOSFET's. (a) Extracted channel profile from the substrate sensitivity of the long-channel devices. The insert shows comparisons between the measured threshold voltages (●) and the calculation of the analytic model (—); (b) Channel length and  $V_{DS}$ -dependences. ● and + are determined from measurements and — and — are calculated by our analytic model.

Similarly,  $f_S$  and  $f_D$  are the integration results of the source/drain boundary potentials with the corresponding weighting functions. Equation (8) is used to compute  $f_S$  and  $f_D$ . The expressions for  $f_S$  and  $f_D$  are

$$f_S = \frac{1}{2} - \frac{1}{3} \frac{y_{do}}{y_{JS}} + \frac{1}{12} \left( \frac{y_{do}}{y_{JS}} \right)^2 \quad (18)$$

and

$$f_D = \frac{1}{2} - \frac{1}{3} \frac{y_{do}}{y_{JD}} + \frac{1}{12} \left( \frac{y_{do}}{y_{JD}} \right)^2 \quad (19)$$

According to (17) and (19), the DIBL factor  $k$  is

$$k \approx a_0 \frac{\pi^2}{2} \frac{\epsilon_S}{\epsilon_{ox}} \frac{T_{ox}}{L} \frac{y_{do}}{L} \left( \frac{R_j}{L} \right)^n f_D \quad (20)$$

The strength of the DIBL effect can be treated as an important performance benchmark for device scaling [18]. As shown by (20), the DIBL factor is proportional to  $\alpha_0 f_D \times (T_{ox}/L) \times (y_{do}/L) \times (R_j/L)^n$  under the long-channel assumption. Eq. (20) can be rearranged to be

$$L_{min} = M [a_0 T_{ox} R_j^n y_{do} f_D]^{1/(2+n)} \quad (21a)$$

where

$$M \equiv \left( \frac{1}{k} \frac{\pi^2}{2} \frac{\epsilon_S}{\epsilon_{ox}} \right)^{1/(2+n)} \quad (21b)$$

is a unitless constant as  $k$  is specified. Note that (21) is valid for nonuniformly doped profile. Since the implant profiles (e.g., double implants) of practical n-MOSFET's need at least six implant parameters, the computer iteration is required for  $y_{do}$  in (21) if the implant profiles in the substrate are known. In order to demonstrate the application of the scaling rule for MOSFET miniaturization, the uniform substrate doping is assumed in the following figures for simplicity. This treatment is similar to those of the constant-field strategy and the empirical laws developed by Brews *et al.* [17] and Ng *et al.* [18].

Fig. 6 illustrates the dependence of the DIBL factor  $k$  on the term  $\alpha_0 f_D \times (T_{ox}/L) \times (y_{do}/L) \times (R_j/L)^n$ . The numerical data points in Fig. 6 begin to deviate significantly from the analytic curve as the assumptions made to derive (16)~(20) are violated, i.e., the long-channel approximation is no longer valid. Consequently, a departure point can be defined to represent the lower limit of channel length below which the long-channel behavior can be maintained. As shown in Fig. 6, the short-channel characteristics become dominant as  $k > 20$  mV/V. Therefore,  $k = 20$  mV/V is a reasonable criterion to distinguish the device performance. For example, for devices with  $N_{AB} = 2 \times 10^{17}/\text{cm}^3$ ,  $T_{ox} = 10$  nm, and  $R_j = 0.10 \mu\text{m}$ ,  $L_{min} = 0.26 \mu\text{m}$  is obtained with  $M = 10.64$ . It is clearly seen that (21) acts as a miniaturization guide, as the empirical law developed by Brews *et al.* [17] does. It's important to note that (21) considers only the DIBL effect. Other requirements may impose other constraints on  $L_{min}$  for the development of a complete design guide. Equation (21) relates the minimum channel length to the three basic structure parameters:  $T_{ox}$ ,  $R_j$ , and  $N_{AB}$ . The term  $y_{do}$  in (21) indicates the requirement of high substrate concentration to achieve device miniaturization. On the other hand, the considerations such as the substrate sensitivity and the parasitic source-to-substrate capacitance play the competing roles for this requirement.

To verify the validity of (21), numerical simulation and experimental data are taken for comparisons.  $L_{min}$  is determined by the method described in Fig. 6 and  $k = 20$  mV/V is used. For numerical simulation, devices with gate oxide thicknesses ranging from 6 to 100 nm, junction depths from 35 nm to  $0.8 \mu\text{m}$ , and uniform substrate doping concentrations from  $3 \times 10^{15}/\text{cm}^3$  to  $2 \times 10^{17}/\text{cm}^3$  were tested. The test devices were fabricated on (100) silicon wafers and the starting material was p-type wafer with the base impurity concentration

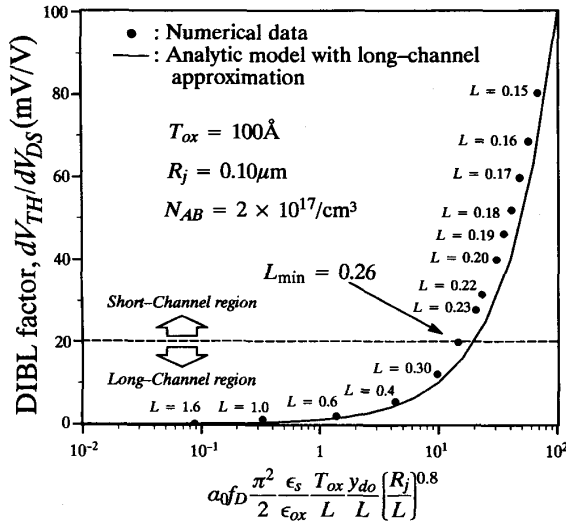


Fig. 6. Determination of minimum channel length  $L_{\min}$  by means of DIBL analysis. The solid curve is predicted by our analytic model with long-channel approximation.  $|dV_{TH}/dV_{DS}| \leq 20$  mV/V is defined to be the requirement of long-channel devices.

of about  $3 \sim 5 \times 10^{15}/\text{cm}^3$ . Ion implantation was used to adjust the substrate doping concentration and the energy was 80 KeV and the dose varied from  $7 \times 10^{11}$  to  $3 \times 10^{14}/\text{cm}^2$ . A long and high temperature annealing process was followed to achieve uniform profile near the surface. The thermal budget was 800°C for 50 min and 1100°C for 590 min. The resulted channel profile was nearly flat to about 1.2  $\mu\text{m}$  depth from the surface. Hence, uniform substrate doping could be assumed and the effective doping concentration was determined from the substrate sensitivity of long-channel MOS devices. Gate oxides with three different thicknesses were grown for 10, 14, and 20 nm and the gate material was  $n^+$ -polysilicon. The source/drain islands are formed by arsenic implantation with 80 keV and  $5 \times 10^{16}/\text{cm}^2$ , and the subsequent annealing for 120 min at about 850°C was carried out and the junction depth is about 0.2  $\mu\text{m}$ .

Fig. 7 summarizes the above verification data, in which the plus signs are extracted from the numerical simulation and the filled circles are from experimental devices. These points fall on a straight line with a slope of 1/2.8 on a log-log plot as predicted by (21). It means that for devices with  $k \leq 20$  mV/V, the punchthrough effect is not significant and hence excellent accuracy can be obtained by our model. Comparisons among various constraint equations will be presented elsewhere [22].

#### IV. CONCLUSION

A new simplified analytic model for the threshold voltage of n-MOSFET's is presented and verified. Given a set of boundary potentials, the averaged normal field derived by Lin and Wu [13] at the Si/SiO<sub>2</sub> interface is successfully applied to the formulation of our model. Careful study on the error-generating mechanisms shows that the major deviation results from the ignorance of the field-retrograde effect [11]. The parameter  $a$  and its corresponding equations correct the errors

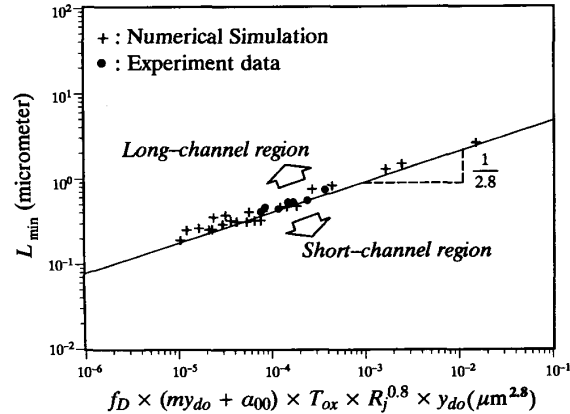


Fig. 7. Relationship between acceptable minimum channel length  $L_{\min}$  and structure parameters.  $L_{\min}$  is defined by the method shown in Fig. 6. The plus signs (+) are determined by 2-D numerical simulation and the filled circles (●) are obtained by experimental measurements. The solid straight line is computed by the new constraint equation  $L_{\min} = M[a_0 T_{ox} R_j^{0.8} y_{do} f_D]^{1/2.8}$  with  $M = 10.64$ .

and reveal several physical pictures of the DIBL effect. The perpetual charge sharing effect is noted and described by the existence of the parameter  $a_{00}$ .

After the successful verification of our model, the DIBL effect is utilized to study the issues of MOSFET miniaturization. By extending our model to the case of uniformly doped substrates and neglecting the charge-screening effect and the depletion-width broadening effect, we derive a new constraint equation similar to the empirical law of Brews *et al.* [17]. Numerical and experimental verifications confirm the validity of the new constraint equation.

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