

STBC-OFDM Downlink Baseband Receiver for Mobile WMAN

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Abstract—This paper proposes a space time block code-orthogonal frequency division multiplexing downlink baseband receiver for mobile wireless metropolitan area network. The proposed baseband receiver applied in the system with two transmit antennas and one receive antenna aims to provide high performance in outdoor mobile environments. It provides a simple and robust synchronizer and an accurate but hardware affordable channel estimator to overcome the challenge of multipath fading channels. The coded bit error rate performance for 16 quadrature amplitude modulation can achieve less than 10^{-6} under the vehicle speed of 120 km/hr. The proposed baseband receiver designed in 90-nm CMOS technology can support up to 27.32 Mb/s uncoded data transmission under 10 MHz channel bandwidth. It requires a core area of $2.41 \times 2.41 \text{ mm}^2$ and dissipates 68.48 mW at 78.4 MHz with 1 V power supply.

Index Terms—Baseband receiver, channel estimator, space time block code-orthogonal frequency division multiplexing (STBC-OFDM) system, synchronizer, wireless metropolitan area network (WMAN).

I. INTRODUCTION

NEXT generation portable Internet services require high data rate and mobile capability to provide various multimedia transmissions. IEEE 802.16e standard which usually refers to mobile worldwide interoperability for microwave access (WiMAX) is an extension of IEEE 802.16–2004 for providing mobility of wireless metropolitan area network (WMAN) [1], [2]. It is based on an orthogonal frequency division multiple access (OFDMA) technique to support multiple access scheme and multiple-input multiple-output (MIMO) systems over multipath fading channels. Space time block code-orthogonal frequency division multiplexing (STBC-OFDM) systems with multiple antennas can provide diversity gains to improve transmission efficiency and quality of mobile wireless systems [3], [4], but accurate channel state information (CSI) is required for diversity combining, coherent detection, and decoding. Moreover, the system performance is also sensitive to the synchronization error. Therefore, high

TABLE I
MAJOR PARAMETERS OF THE PROPOSED STBC-OFDM SYSTEM

Parameters	Values
RF frequency	2.5 GHz
System channel bandwidth (BW)	10 MHz
Sampling frequency (F_s)	11.2 MHz
Sampling factor	28/25
FFT size (N)	1024
Subcarrier spacing (Δf)	10.9 kHz
Useful symbol time (T_b)	91.4 μ s
Guard time (T_g)	11.4 μ s
OFDM symbol duration (T_s)	102.9 μ s
Number of OFDM data symbols in a DL sub-frame	40
DL	Number of pilot subcarriers (N_{Pilot})
	120
PUSC	Number of data subcarriers (N_{Data})
	720

quality synchronization and channel estimation are two crucial challenges for realizing a successful STBC-OFDM system in outdoor mobile channels.

In this paper, an STBC-OFDM downlink baseband receiver for mobile WMAN is proposed and implemented. First, a novel match filter is proposed to precisely detect symbol boundary. Moreover, a ping-pong algorithm is presented to improve the performance of carrier frequency synchronization [5]. Then, we propose a two-stage channel estimator to accurately estimate CSI over fast fading channels [6]. The initialization stage uses discrete Fourier transform (DFT)-based channel estimation with the multipath interference cancellation (MPIC)-based decorrelation to identify significant channel paths [7], [8]. The tracking stage uses decision-feedback (DF) DFT-based channel estimation with Newton's method [9], [10] to track the gain variations of these paths. The proposed baseband receiver designed in 90-nm CMOS technology can support up to 27.32 Mbps downlink (uncoded) data transmission under 10 MHz channel bandwidth. This design has a core area of $2.41 \times 2.41 \text{ mm}^2$ and dissipates 68.48 mW at 78.4 MHz operating frequency. This paper includes the following features:

- provision of a STBC-OFDM downlink baseband receiver architecture that is capable of high-speed transmission at high mobility;
- integration of a simple and robust synchronizer and an accurate but hardware affordable channel estimator to overcome the challenge of outdoor fast fading channel;
- implementation of a successful STBC-OFDM downlink baseband receiver for mobile WMAN.

This paper is organized as follows. Section II introduces the proposed system architecture. The proposed baseband receiver is then described in Section III. Section IV presents the architecture and circuit design. Then, the simulation and implementation results are provided in Section V. Finally, Section VI is the conclusions.

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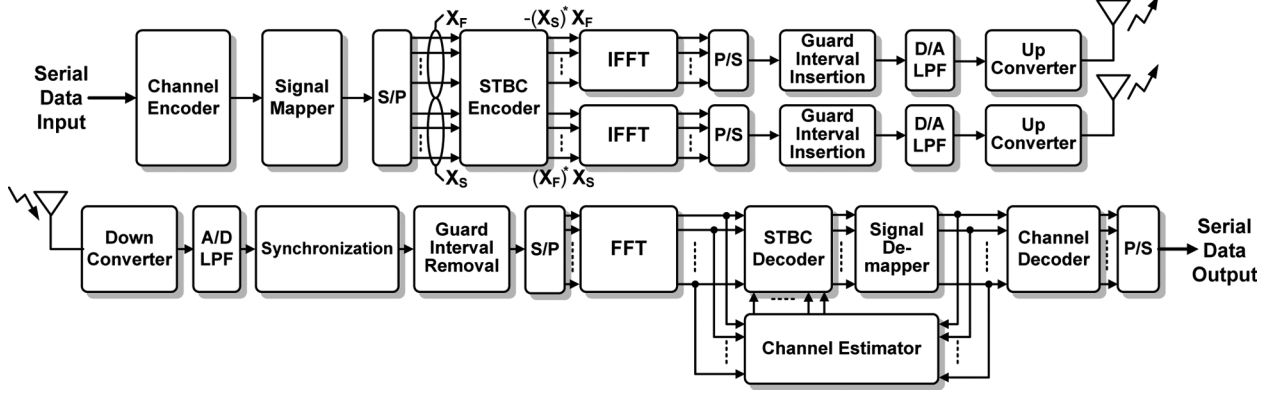


Fig. 1. Proposed STBC-OFDM system with two transmit antennas and one receive antenna.

II. SYSTEM ARCHITECTURE

The proposed STBC-OFDM system is based on IEEE 802.16e OFDMA specification and supports the distributed subcarrier allocation of partial usage of subchannels (PUSC) for downlink (DL) transmission. The major parameters are summarized in Table I. The fast Fourier transform (FFT) size (N) is set to 1024. The length of cyclic prefix (CP) is 128 sampling periods. The modulation schemes of quadrature phase shift keying (QPSK) and 16quadrature amplitude modulation (16QAM) are supported for data subcarriers, while binary phase shift keying (BPSK) is adopted for pilot subcarriers and preamble symbols. A DL sub-frame is composed of one preamble symbol and 40 OFDM data symbols. The system design target is to support carry frequency offset (CFO) up to ± 14 ppm and is optimized to enable the vehicle speed up to 120 km/hr. The maximum Doppler frequency f_d is about 0.025 (normalized to a subcarrier spacing). The coherence time T_c calculated by a typical way [11] is $0.423/f_d = 1.5$ ms which is about 14.8 times of an OFDM symbol time but is smaller than a frame time. Therefore, the channel can be treated as quasi-static within several symbol times but may vary a lot during one frame transmission.

Fig. 1 shows the proposed STBC-OFDM system with two transmit antennas and one receive antenna. In the transmitter, serial data first pass through the constellation mapper and then pass through serial-to-parallel (S/P) to form two transmitted symbols during a time slot which is equivalent to two OFDM symbol times. These two transmitted symbols are encoded by Alamouti's STBC scheme [3], transformed by N -point inverse fast Fourier transform (IFFT), and inserted with a guard interval T_g to prevent inter-symbol interference (ISI). A complete OFDM symbol with the symbol duration $T_b + T_g$ is transferred to an analog signal by a digital-to-analog (D/A) converter, filtered by a low-pass filter (LPF), up converted to RF band, and transmitted. The signal is received from an antenna, down converted to the baseband, low-pass filtered, and digitized by an analog-to-digital (A/D) converter. The proposed baseband receiver consists mainly of two parts: synchronizer and channel estimator. The channels are assumed to be quasi-static within any two successive OFDM symbol durations. Hence, without loss of generality, the received signal processing is focused on each time slot, which is two OFDM symbol times, and the time

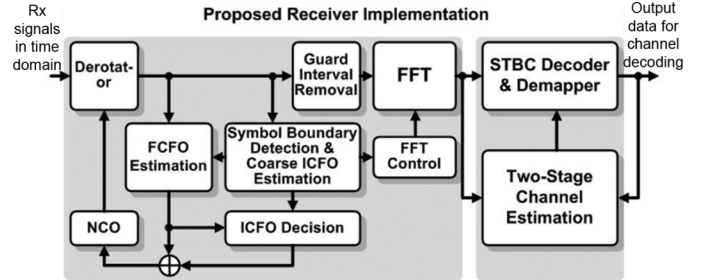


Fig. 2. Architecture of the proposed downlink baseband receiver.

index of symbol transmission is omitted hereafter except otherwise mentioned.

III. PROPOSED BASEBAND RECEIVER DESIGN

Fig. 2 shows the architecture of the proposed downlink baseband receiver. The proposed receiver includes a symbol boundary detector, an integer carrier frequency offset (ICFO) estimator, a fractional carrier frequency offset (FCFO) estimator, an FFT, a two-stage channel estimator, an STBC decoder, and a demapper.

A. Simple and Robust Synchronization

Synchronization includes symbol timing, sample clock, and carrier frequency synchronization. The proposed synchronizer concentrates on the symbol boundary detection and the carrier frequency recovery loop as presented in the following sections.

1) *Symbol Boundary Detection*: An ISI free region of symbol timing detection is determined by the difference in length between the CP and the channel impulse response [12]. Since the proposed system has two transmit antennas, the signals transmitted from different antennas may arrive at the receiver with different delays due to multipath effect. Therefore, the decided boundary must locate in the common ISI free region to prevent the respective ISI effects from other symbols. IEEE 802.16e standard provides three types of preamble subcarrier sets which can be expressed as [2]

$$\text{PreambleCarrierSet}_s = s + 3 \cdot k \quad (1)$$

where $s = 0, 1$, and 2 is the subcarrier set index, and k denotes a running subcarrier index. These subcarriers are modulated

by BPSK with a specific pseudo-noise (PN) code. Because the FFT size is not a multiple of 3, the time-domain preamble symbol is not exactly periodic. Using delay correlation method is difficult to precisely detect symbol boundary. Since the preamble symbol is a known sequence after system acquisition, a match filter corresponding to the time-domain preamble sequence $p^{(i)}[m]$ transmitted from i th antenna can be applied to match the received sample sequence $r[n]$ and obtain the symbol boundary $s^{(i)}$. The match filter complexity depends on the matching length, so a suitable length (L) must take both performance and complexity into consideration. The symbol boundary $s^{(i)}$ can be found as

$$s^{(i)} = \max_n \left(\sum_{m=0}^{L-1} r[n+m] \cdot \left(p^{(i)}[m] \right)^* \right) \quad (2)$$

where n and m denote the sample indices. When the index n corresponds to the peak of the matching results, the value of $s^{(i)}$ will be found. According to the values of $s^{(i)}$, $i = 1$ and 2 , the final symbol boundary is decided to be located in the common ISI free region.

However, the mismatch of oscillator frequency in a receiver and a transmitter causes frequency offset effects in the received signals and destroys the characteristic of the matching results. In order to overcome this problem, we propose a modified match filter. The filter coefficient sequence which is the known preamble sequence is compensated with the possible values of ICFO. An output peak will appear in matching with the preamble sequence compensated with the corresponding ICFO. Hence, this match filter has an additional advantage that the coarse ICFO can be detected simultaneously. The proposed design is defined to support the frequency offset to ± 14 ppm variation. The maximum CFO is equivalent to ± 35 kHz in 2.5 GHz carrier frequency. Therefore, there are seven possible ICFO values ranging +3 to -3.

2) *Carry Frequency Recovery*: After symbol boundary has been successfully obtained, the CP position is known. The CP repeating characteristic can be used to estimate FCFO by correlating the CP with the corresponding received sample sequence. However, when the CFO value is in the middle of two integer values, the accuracy of ICFO detection by using the match filter method is substantially decreased. Because the ICFO effects caused by these two integer values are almost the same, there are two undistinguishable peaks in the matching results. The undistinguishable peaks caused by noise and another antenna interference may easily result in wrong ICFO detection. Therefore, a ping-pong algorithm is proposed to improve the performance of ICFO detection. The ping-pong algorithm partitions each CFO region into the strong region and the weak region depending on the distance to each integer value, as shown in Fig. 3. The accurately estimated FCFO value can be used to correct the ICFO detection. When the estimated FCFO value locates in the strong region, the matching results have strong reliability to determine ICFO by detecting the peak value. When the estimated FCFO value locates in the weak region, there are two possible peaks in the matching results. Thus, the ICFO value will be adjusted by the information of the FCFO value and these two peaks. For example, there are two peaks appearing in the ICFO values of

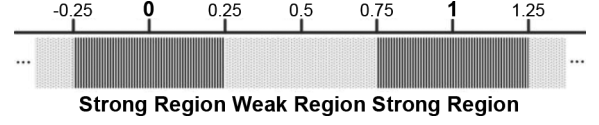


Fig. 3. CFO region partition for the proposed ping-pong algorithm.

0 and 1, and the FCFO value is correctly estimated to be 0.4 located in the weak region. If the ICFO value is detected to be 1 directly depending on the output peak, the estimated CFO is 1.4. This result is unreasonable because another peak is 0 but not 2. By using this ping-pong algorithm, the ICFO value will be correctly adjusted to be 0.

The error probability of ICFO detection is simulated at the vehicle speed of 60 km/hr with E_b/N_0 of 16 dB, where E_b/N_0 is a ratio of the received bit energy to the noise power spectral density. The error probability using the direct detection method rapidly increases to about 0.5 when FCFO approaches 0.5 (the weak region), whereas it is normally about 10^{-3} . However, the proposed ping-pong scheme is effective to maintain ICFO error probability at about 10^{-3} in the weak region.

B. Accurate Two-Stage Channel Estimation

Two major categories of pilot-aided channel estimation methods are interpolation-based channel estimation methods [13], [14] and DFT-based channel estimation methods [7], [8]. Interpolation-based method estimates channel frequency response (CFR) by interpolating the received pilot subcarriers. This method is not suitable for outdoor fast fading channels. This is because the channel coherent bandwidth becomes small, and using the interpolation-based method with limited pilot information becomes more difficult to recover channel variations. DFT-based method focuses on transform domain to characterize time-domain channel impulse response (CIR) and effectively improves the performance by suppressing time-domain noise. Many DFT-based methods derived from maximum likelihood (ML) scheme have been studied for OFDM systems with preambles [7], [8]. In order to further improve the estimation performance, the DF DFT-based channel estimation method is employed by using decided data subcarriers as pilot subcarriers to track channel variations for saving transmission bandwidth and providing sufficient tracking information [9].

A two-stage channel estimation method is used to realize a successful STBC-OFDM system in outdoor mobile channels. The multipath fading channel is characterized by CIR consisting of a few significant paths. The delays of these paths usually vary slowly in time, but the path gains may vary relatively fast. Therefore, in the initialization stage, the significant paths are identified during the preamble symbol time. In the tracking stage, the path gain variations in the identified path positions will be tracked in the following data symbol transmission. Fig. 4 shows the architecture of the two-stage channel estimator.

1) *Initialization Stage*: The operation blocks in this stage are a preamble match, an IFFT, a straight multipath interference cancellation (SMPIC)-based decorrelator, and an FFT. The preamble match correlates the received signal with the frequency-domain preamble symbol to get the preliminary CFRs of different antenna pairs. Then, the CIR $m^{(i)}[\tau]$ can be obtained

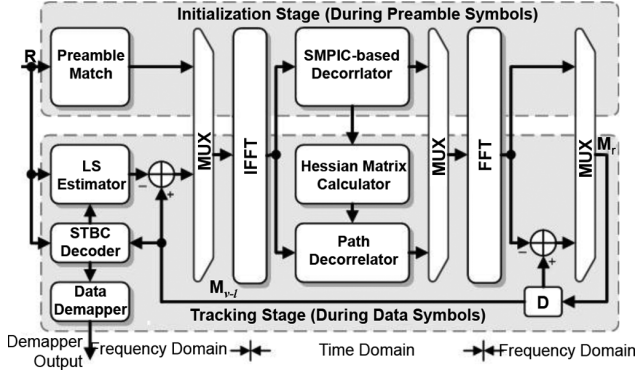


Fig. 4. Block diagram of the proposed two-stage channel estimator.

by IFFT operation, where τ denotes the path delay index, and i is the transmit antenna index. Since there are null tones in the preamble symbol, the interference between the CIR paths occurs. An SMPIC-based decorrelator is used to identify significant paths and cancel the multipath interference which can be calculated by the known time-domain preamble sequence. Two parameters N_P and N_B are defined as a presumptive CIR path number and the observation length, respectively. If the CIR are path-by-path picked out and decorrelated from $m^{(i)}[\tau]$ for $0 \leq \tau < N_B$, this process requires the execution cycles of about $O(N_P N_B \log_2 N_B)$ that is too costly to implement the hardware with a limited timing budget. Therefore, a straightforward SMPIC-based method is proposed, and the procedures are listed as follows.

- 1) Sort the N_B paths to find the first $\beta \cdot N_P$ paths with large path gain of $m^{(i)}[\tau]$, where β is an integer.
- 2) Carry out from the largest to the smallest one of these $\beta \cdot N_P$ paths to cancel the path interference.
- 3) Sort these decorrelated $\beta \cdot N_P$ paths to pick up the first N_P paths.

To minimize the implementation cost while keeping an acceptable performance, the β value can be evaluated by the output signal-to-noise ratio (SNR) of data decision results [6]. The SMPIC-based method only requires $O(N_B \log_2 N_B)$ execution cycles that are reduced by about $O(N_P)$ times as compared to the path-by-path decorrelation method. Finally, these identified paths are transformed back to CFR by FFT.

2) *Tracking Stage*: The operation blocks in this stage are an STBC decoder, a data demapper, a least-square (LS) estimator, an IFFT, a Hessian matrix calculator, a path decorrelator, and a FFT. To have the fine local optimization capability for estimating time-varying channels, the DF DFT-based channel estimation method combining with Newton's method is adopted [10]. First, the STBC decoder is based on the last estimated CFRs to decode the first and second received symbols in a time slot, $X_F[k]$ and $X_S[k]$, where k denotes the subcarrier index. Then, the LS estimation vector $\epsilon_v = \{\epsilon_v^{(i)}[k] : i = 1, 2\}$ for $k \in \Theta$ are calculated by the LS estimator and given as

$$\epsilon_v[k] = (\mathbf{X}[k])^* \frac{\mathbf{R}[k]}{C_v[k]} \quad (3)$$

$$\mathbf{X}[k] = \begin{bmatrix} X_F[k] & -(X_S[k])^* \\ X_S[k] & (X_F[k])^* \end{bmatrix} \quad (4)$$

where Θ is the data subcarrier set, $\mathbf{R}[k] = \{R[t, k] : t = 1, 2\}$ is the received symbol vector in a time slot, t is symbol index, v is the running iteration index, and $C_v[k] = |X_F[k]|^2 + |X_S[k]|^2$ is the energy normalized factor. The LS estimations at pilot subcarriers $\epsilon_v^{(i)}[k]$ for $k \in \mathbf{J}$ can be obtained by dividing the received pilot by the corresponding pilot value, where $\mathbf{J}$ is the pilot subcarrier set. The offset vector $\Delta_v[k] = \{\Delta_v^{(i)}[k] : i = 1, 2\}$ is acquired by

$$\Delta_v[k] = \mathbf{M}_{\nu-1}[k] - \epsilon_v[k] \quad (5)$$

where $\mathbf{M}_{\nu-1}[k] = \{M_{\nu-1}^{(i)}[k] : i = 1, 2\}$ is the last estimated CFR vector. The gradient vector $\mathbf{q}_\nu^{(i)} = \{q_\nu^{(i)}[\tau] : \tau \in \Lambda^{(i)}\}$ used in Newton's method can be obtained by

$$\mathbf{q}_\nu^{(i)} = \text{IDFT} \left\{ \Delta_\nu^{(i)}[k] : k \in \Theta \cup \mathbf{J} \right\} \quad (6)$$

where $\Lambda^{(i)} = \{\tau_0^{(i)}, \dots, \tau_{N_P}^{(i)}\}$ is the significant path-delay set that is identified in the initialization stage, and $\text{IDFT}\{\cdot\}$ denotes inverse DFT (IDFT) process. Since only the gradients at the significant paths will be processing, white noise is filtered out, and the decision error propagation effect can also be alleviated. However, the subcarrier locations are not equally-spaced, so there are the aliasing among the estimated paths. The path decorrelation can be formed by multiplying the gradient vector with the $N_P \times N_P$ weighting matrix $[\mathbf{E}^{(i)}]^{-1}$ which is the inverse of the Hessian matrix used in Newton's method [6], [10]. The (l, l') th entry of $\mathbf{E}^{(i)}$ is given by

$$(\mathbf{E}^{(i)})_{l, l'} = \sum_{k \in \Theta} \cos \left(\frac{2\pi k (\tau_l^{(i)} - \tau_{l'}^{(i)})}{N} \right) + j \sum_{k \in \Theta} \sin \left(\frac{2\pi k (\tau_l^{(i)} - \tau_{l'}^{(i)})}{N} \right) \quad (7)$$

for $\tau_l^{(i)}, \tau_{l'}^{(i)} \in \Lambda^{(i)}$. The decorrelated frequency-domain gradients $\delta_v^{(i)} = \{\delta_v^{(i)}[k] : k \in \Theta \cup \mathbf{J}\}$ can be expressed as

$$\delta_v^{(i)} = \text{DFT} \left\{ [\mathbf{E}^{(i)}]^{-1} \mathbf{q}_\nu^{(i)} \right\} \quad (8)$$

where $\text{DFT}\{\cdot\}$ indicates DFT process. The new estimated CFR vector $\mathbf{M}_\nu[k] = \{M_\nu^{(i)}[k] : i = 1, 2\}$ is obtained by compensating the previous estimated CFR vector $\mathbf{M}_{\nu-1}[k]$ with $\delta_v[k] = \{\delta_v^{(i)}[k] : i = 1, 2\}$, as given by

$$\mathbf{M}_\nu[k] = \mathbf{M}_{\nu-1}[k] - \delta_v[k]. \quad (9)$$

However, the matrix inverse computing of $[\mathbf{E}^{(i)}]^{-1}$ requiring massive complex multiplications must be avoided for hardware implementation. Therefore, the strongly diagonal property [15] is used to approximate $[\mathbf{E}^{(i)}]^{-1}$ as

$$\begin{aligned} [\mathbf{E}^{(i)}]^{-1} &= \frac{1}{N_\Theta} (\mathbf{I}_{N_\Theta} + \mathbf{O}_{\text{off}})^{-1} \\ &\approx \frac{1}{N_\Theta} (\mathbf{I}_{N_\Theta} - \mathbf{O}_{\text{off}}) \\ &= \frac{1}{N_\Theta^2} (2N_\Theta \mathbf{I}_{N_\Theta} - \mathbf{E}^{(i)}) \end{aligned} \quad (10)$$

TABLE II
WORD LENGTHS OF SEVERAL KEY SIGNALS IN THE PROPOSED RECEIVER

Signal	Word Length	Signal	Word Length
Received Sample Input	10	Preamble Match Output	12
CORDIC Input	14	LS Estimator Output	14
CORDIC Output	14	STBC Decoder Output	9
FFT Output	13	IFFT/FFT Output	16
FFT Twiddle Factor	18	SMPIC Decorrelator Output	14
Channel Response Output	16	Path Decorrelator Output	14

where N_Θ is the dimension of Θ , $\mathbf{I}_\kappa$ is a $N_P \times N_P$ identity matrix, and $\mathbf{O}_{\text{off}}$ is a zero-diagonal matrix.

We take the hardware implementation and performance issues into the consideration in the algorithm and system development. The proposed baseband receiver design has the following features.

- The proposed match filter applied with the ICFO-compensated coefficients can reduce the CFO effect and provide the precise symbol boundary detection, and the ICFO value can be detected simultaneously.
- The proposed ping-pong algorithm using the estimated FCFO value can refine the ICFO value and improve the accuracy.
- The proposed two-stage channel estimation can highly improve the performance in outdoor mobile channels as compared with the interpolation-based methods that are frequently adopted in the baseband implementation.
- In the initialization stage, the proposed SMPIC-based decorrelator uses a straightforward method to identify significant paths and cancel the multipath interference, which can highly reduce the implementation cost.
- In the tracking stage, the matrix inverse computation is efficiently avoided by employing the strongly diagonal property, which can highly save the computation complexity.

IV. ARCHITECTURE AND CIRCUIT DESIGN

The decision of signal word lengths affects the system performance and hardware complexity. The output SNR at the STBC decoder is used as a performance criterion to determine the appropriate word lengths of each building block. The word lengths of several key signals in the proposed receiver are summarized in Table II.

A. Synchronizer

In the match filter, each tap performs complex multiplication of the coefficient and the received sample. If the coefficients are quantized into $\{-1, 1\}$ [16], the tap operation can be simplified to add or subtract the received sample. It avoids the multiplier usage and reduces the register requirement. However, the sign calculation is necessary due to subtraction, and more hardware effort is required for sign extension. Therefore, if the signed calculation is avoided, the hardware and power will be further saved. In the proposed method, both the real and imaginary parts of the received sample are quantized into $\{-1, 0, 1\}$. The quantization loss is less than 0.8 dB in SNR, and it can be compensated by increasing the matching length L , which costs only a little hardware overhead. When the total numbers of 0's and 1's stored in tap registers, denoted as N_0 and N_1 , are known, the

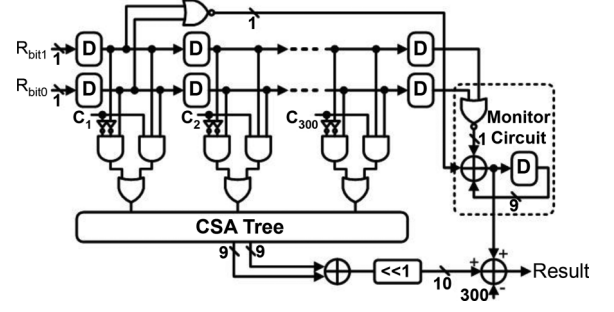


Fig. 5. Block diagram of the proposed match filter.

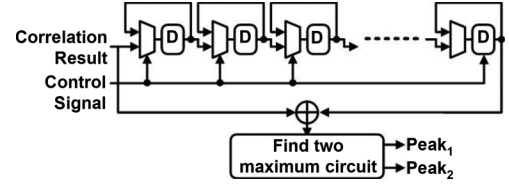


Fig. 6. Storage units for storing the previous matching results.

number of -1 's can also be obtained at the same time. Therefore, the matching result can be calculated as

$$\text{Matching Result} = N_1 - (L - N_0 - N_1) = 2N_1 - L + N_0. \quad (11)$$

According to the simulation results at the vehicle speed of 120 km/hr, the matching length of 300 is chosen in this case so that the symbol miss error probability approaches the lowest boundary. The match filter design is shown in Fig. 5. A monitor circuit is used to count N_0 after each data updating. The tap results are generated by the logical circuits and are accumulated to obtain N_1 by a carry save adder (CSA) tree. A logical circuit can be simplified to use only NAND gate and NOR gates. In the proposed symbol boundary detection, the coefficient sequence is pre-shifted with the possible values of ICFO, so the ICFO can be detected simultaneously. The coefficient sequence is stored in ROM. In order to accumulate the matching results twice for ICFO detection, an additional circuit is necessary to store the previous matching results as shown in Fig. 6. If the control signal is positive, the registers will respectively store the current matching results of the possible ICFO values. On the contrary, if a control signal is negative, the chain of the registers works as the shift-registers for accumulating the matching results. Finally, the accumulated results are passed to the comparator to select the two ICFO values that have maximum peaks in the accumulated results.

Fig. 7 shows the cross correlation circuit for the FCFO estimation, and the FCFO estimate is derived from the phase of this complex correlation output. In FCFO estimation, a 1024 delay-line is necessary to store the received data and to do the correlation. Shift registers for realizing the delay-line will cost a lot of area and power consumptions. A twister memory operation presented in [17] is used to reduce the cost of memory area. Besides, the complex multiplier can be realized from four multipliers and two adders to three multipliers and five adders.

To derive the phase of the complex correlation output, an arctangent function can be implemented by the coordinate ro-

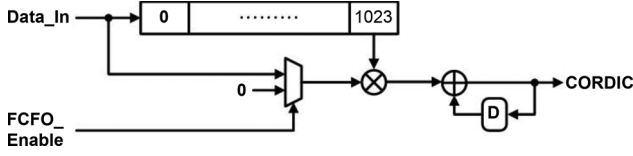


Fig. 7. Cross correlation circuit for the FCFO estimation.

tation digital computer (CORDIC) circuit [18]. Moreover, the CORDIC circuit can also be used to provide the values of sine and cosine for derotating the CFO effect.

B. Two-Stage Channel Estimator

The operation of the proposed channel estimator (see Fig. 4) contains the initialization stage and the tracking stage. The FFT/IFFT module can be shared between these two stages.

1) *Initialization Stage*: The preamble match is used to estimate preliminary CFRs. The preamble subcarrier values are boosted as a constant power. To avoid the multiplier usage in matching calculation, the absolute value of the normalized preamble subcarrier can be expressed as a constant canonic signed digit (CSD) code [19]. The preamble match design only requires adders and multiplexers controlled by the sign of the preamble patterns. Thus, only the sign bits of the preamble patterns are stored. The SMPIC-based decorrelator is used to identify the significant paths in a straightforward method. In this design, N_B is 128 and is same as the CP length, and N_P is presumed to be eight. Based on the output SNR evaluation at the vehicle speed of 120 km/hr, the β value is decided to be four. The SMPIC-based decorrelator consists of a partial sorting network and a decorrelator. An 8-item sorter arranged with eight memory modules are used for partial sorting [20] as shown in Fig. 8. The sorter is based on the Batcher's sorting network [21], and the basic unit is a 2×2 comparator which is used to perform data comparison and exchange. The memory modules are used to store the path power values. The merge sorting procedure is used two times to sort the 128-to-32-item data and the 32-to-8-item data. After the first sorting, the decorrelator starts to cancel the path interference in iterative way starting from the first legal path with the maximum sorted path gain

$$\mu_\rho = \tilde{\mu}_\rho - \mu_\kappa C_{PP}[\tau_\rho - \tau_\kappa], \quad \kappa < \rho \leq 31, \quad 0 \leq \kappa < 31 \quad (12)$$

where μ_κ is the κ th legal path gain, $\tilde{\mu}_\rho$ is the ρ th sorted path gain, μ_ρ is the ρ th decorrelated sorted path gain, τ_κ is the κ th legal path delay, τ_ρ is the ρ th sorted path delay, and $C_{PP}[\tau]$ is the normalized cyclic auto-correlation of the preamble symbol. At the κ th iteration, the interference associated with the κ th legal path will be cancelled. The κ th path interference as compared with previous $(\kappa - 1)$ legal path gains is too small to affect the significant path decision and can be revised in the tracking stage without performance loss. Therefore, the process does not cancel the interference to previous $(\kappa - 1)$ paths to save half of execution cycles and power consumption. The value of $C_{PP}[\tau]$ can be pre-calculated and stored in ROM.

2) *Tracking Stage*: By using dividers, the STBC decoder can be implemented intuitively. However, a divider is very costly. By operating with the two-stage dichotomy demapping method

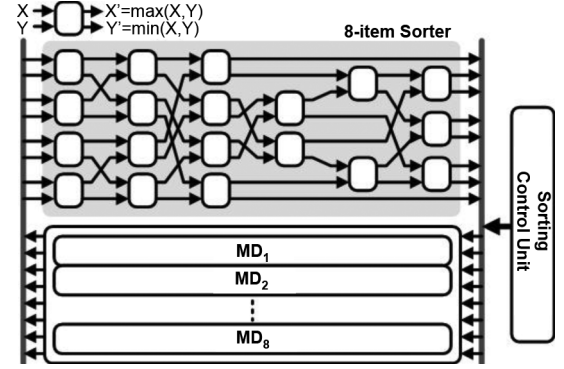


Fig. 8. Block diagram of the partial sorting network.

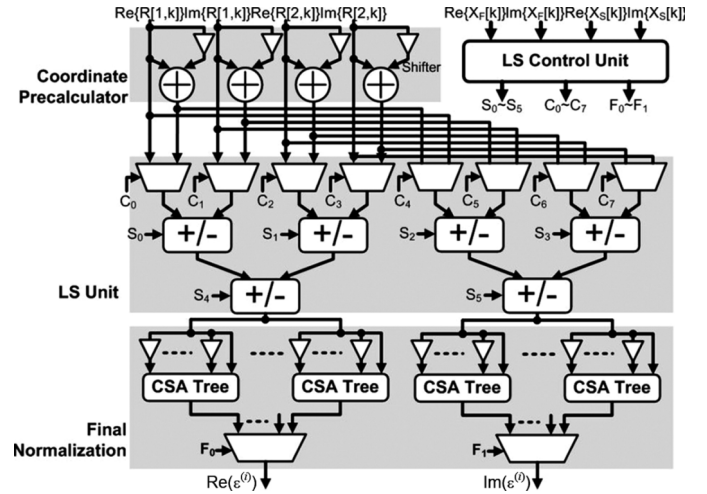


Fig. 9. Design of the LS estimator.

[22], the divisions can be avoided by scaling the constellation with the normalized term of the STBC decoding.

The LS estimator contains a coordinate precalculator, an LS unit, an LS control unit, and a final normalization, as shown in Fig. 9. The coordinate precalculator is hardwired to get the results of $R[t, k]$ multiplied by the coordinate values of $X_F[k]$ and $X_S[k]$. An LS unit which consists of multiplexers and adders computes the LS estimations without normalization. Since both the constellation normalization and $1/C_v[k]$ values have a limited constant set, the final normalization can be implemented by a limited-set of CSD multiplications without using a divider. According to the coordinate values of $X_F[k]$ and $X_S[k]$, the LS control unit will generate the corresponding control signals.

In the path decorrelation, the complex multiplications of the order $O(N_P^3)$ for the Hessian matrix inverse $[\mathbf{E}^{(i)}]^{-1}$ are effectively saved by considering the strongly diagonal property. Nevertheless, for each entry calculation, we still require a lot of cycles to sum the cosine and sine values by using a lookup table. The online computation of $[\mathbf{E}^{(i)}]$ has at least $O(2N_P^2 \cdot N_\Theta)$ additions and requires the storage for sinusoidal table lookup, where N_Θ is the dimension of Θ . Besides, the path decorrelation, $[\mathbf{E}^{(i)}]^{-1} \mathbf{q}_v^{(i)}$, requires $O(N_P^2)$ complex multiplications and complex additions. However, we observe that inter-path interference degrades dramatically when $|\tau_l^{(i)} - \tau_{l'}^{(i)}|$ gradually becomes large. After the quantization, most of entry values of

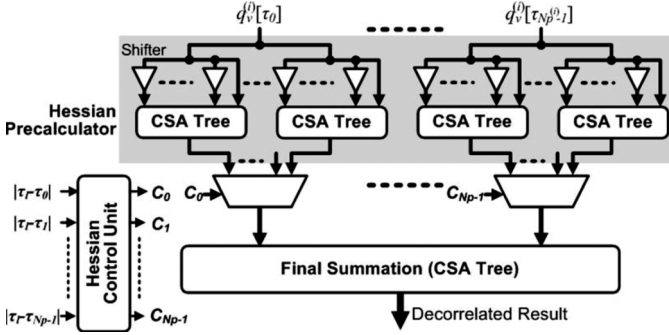


Fig. 10. Design of the path decorrelator.

$[\mathbf{E}^{(i)}]^{-1}$ become zero, so the nonzero quantized entry values can be expressed in CSD codes and optimized for their common subexpressions [23]. The path decorrelation $[\mathbf{E}^{(i)}]^{-1} \mathbf{q}_v^{(i)}$ can be implemented by hardwired CSD multiplications, and the online computation of $E^{(i)}$ is also avoided.

The path decorrelator is composed of a Hessian precalculator, a Hessian control unit, multiplexers, and a final summation, as shown in Fig. 10. The Hessian precalculator is used to multiply $\mathbf{q}_v^{(i)}$ with the nonzero values of $[\mathbf{E}^{(i)}]^{-1}$ and is only executed once during the path decorrelation. The Hessian control unit is based on the $|\tau_l^{(i)} - \tau_{l'}^{(i)}|$ value to select the corresponding results for final summation. Finally, the final summation outputs the decorrelated $\mathbf{q}_v^{(i)}[\tau_\kappa]$, $0 \leq \kappa \leq N_P - 1$. Based on the proposed architecture, the path decorrelation just requires at most $O(N_P \cdot (N_P + N_E))$ complex additions, where N_E is the nonzero digit number of all possible entry values of $[\mathbf{E}^{(i)}]^{-1}$.

C. FFT/IFFT

The FFT and IFFT are required by the proposed two-stage channel estimator and can be shared by the initialization stage and the tracking stage. A parallel memory-based FFT/IFFT architecture with multiple inputs and outputs in normal order is used to have a lower cost and reduce the latency which is targeted to be less than 1/4 of an OFDM symbol time. Fig. 11 shows the 1024-point FFT/IFFT module that is composed of eight independent memory modules, four radix-8 processing elements (PEs), two radix-2 butterfly elements, and two commutators. The memory modules are implemented with single-port SRAM modules which consume less area and power than dual-port SRAM modules. The PE adopts the pipelined single-path delay feedback (SDF) FFT architecture with a reorder buffer [24], [25], a complex multiplier and the associated twiddle factor table, as shown in Fig. 12. By the symmetry property of sine/cosine functions, the lookup table just requires to store the sine/cosine values from 0 to $\pi/4$.

For radix-8 FFT operation, the read-out data index of the memory access is the 3-bit reversal of the write-in data index. In order to achieve the parallel inputs and outputs in normal order, the memory access addressing for eight memory modules must avoid the memory conflict occurring. Assume that the binary index of the write-in data is $\{A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0\}$, and the binary index of the read-out data is $\{B_9 B_8 B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0\}$. A data in the read-out index $\{B_9 B_8 B_7 B_6 B_5 B_4 B_3 B_2 B_1 B_0\}$ mapping to the

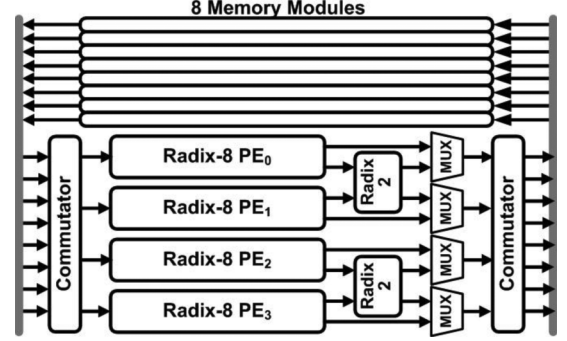


Fig. 11. Radix-8 1024-point parallel memory-based FFT architecture.

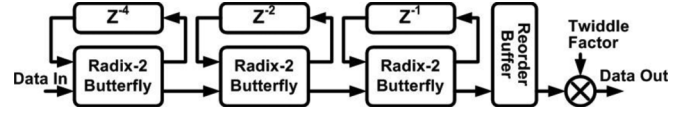


Fig. 12. Radix-8 processing element.

3-bit reversal write-in index is $\{A_2 A_1 A_0 A_5 A_4 A_3 A_8 A_7 A_6 A_9\}$. The parallel write-in data assigned to the eight independent memory modules are based on the addressing scheme of $\{A_2 A_1 A_0\} + \{A_9 A_8 A_7\}$. The data located in the different memory modules can be parallel outputted in normal order.

D. Data Flow

In the proposed baseband receiver, the time-domain OFDM symbols after phase compensation are passed through the FFT processor for OFDM demodulation. The frequency-domain OFDM symbols are then passed to the channel estimation and STBC decoding modules. Since the STBC-OFDM system has two transmit antennas and one receive antenna, two received OFDM symbols in a time slot must be ready at the same time for channel estimation and STBC decoding. Thus, the FFT processor along with five memory banks, MB_R1_0, MB_R1_1, MB_R1_2, MB_R2_0, and MB_R2_1, are used to perform OFDM demodulation and buffer the received OFDM symbols as shown in Fig. 13. After phase compensation, a time-domain OFDM symbol is written into one of these five memory banks for FFT processing. While FFT processing, the time-domain received OFDM symbol is continuously written to another memory bank. After two OFDM symbols in a time slot have been FFT transformed, the memory banks storing these two OFDM symbols are ready for the access from channel estimation and STBC decoding. The process of channel estimation and STBC decoding must be finished within a time slot. The memory banks MB_R1_0, MB_R1_1 and MB_R1_2 are used to buffer the first received OFDM symbol in a time slot. The memory banks MB_R2_0 and MB_R2_1 are used to buffer the preamble symbol and the second received OFDM symbol in a time slot.

The flow chart of the proposed receiver is shown in Fig. 14. After phase compensation, the preamble symbol is first written to MB_R2_0, but MB_R1_2 is no access. The following two OFDM symbols are then written to MB_R1_0 and MB_R2_1 while the preamble symbol in MB_R2_0 are calculated by FFT

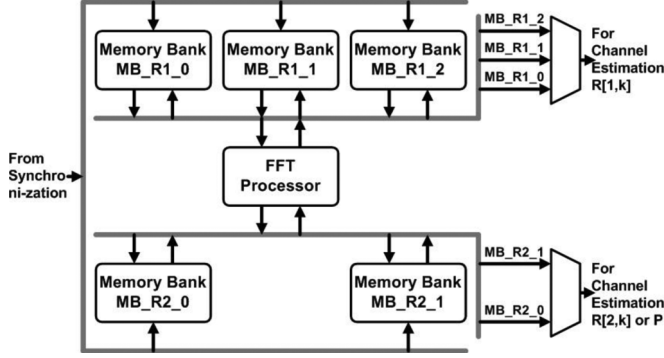


Fig. 13. FFT processor arranged with five memory banks.

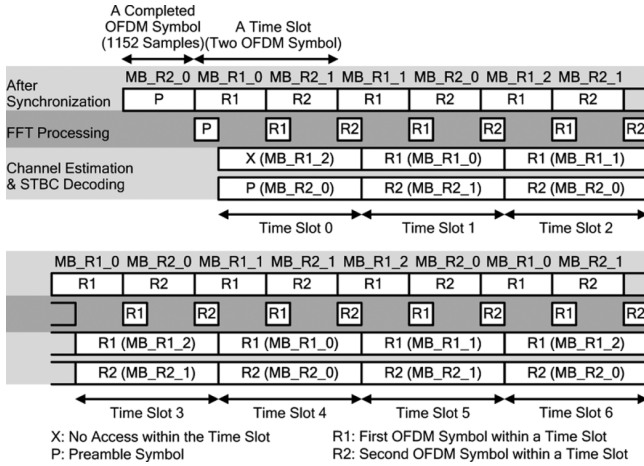


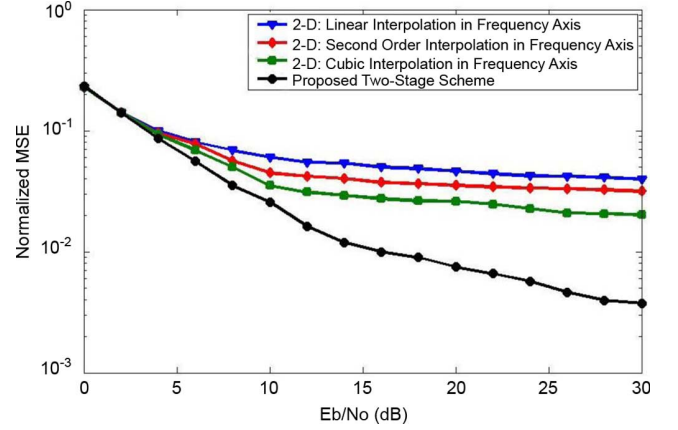
Fig. 14. Flow chart of the proposed receiver.

processor and then ready at the time slot 0 for the channel estimation and STBC decoding access. Similarly, when the other two OFDM symbols are written to MB_R1_1 and MB_R2_0, the two OFDM symbols in MB_R1_0 and MB_R2_1 are ready at the time slot 1. Following the flow chart, the access scheme of MB_R1_2 and MB_R2_0 at the time slot 6 is similar as that at the time slot 0, but the written data are two OFDM symbols in a time slot. The memory access schemes of these five memory banks are repeated every six time slots.

V. EXPERIMENTAL RESULTS

The performances of the proposed baseband receiver are demonstrated through fixed point simulations of the proposed system with two transmit antennas and one receive antenna. The carrier central frequency is set to 2.5 GHz with CFO to be ± 14 ppm. The multipath fading channel uses the International Telecommunication Union (ITU) Veh-A [26] channel model with relative path power profiles of 0, -1, -9, -10, -15, and -20 (dB), and the path excess delays are uniformly distributed from 0 to 50 sample periods. Moreover, Jakes' model is used to generate the Rayleigh fading in the vehicle environment [27].

We provide simulations of the STBC-OFDM system that adopts 2-D interpolation channel estimation methods to make the performance comparison. These methods perform linear interpolation among contiguous time slot in time axis and linear, second order, and cubic interpolations in frequency axis, respectively [13], [14]. Fig. 15 shows the normalized

Fig. 15. Normalized MSE of channel estimation at ν_e of 120 km/hr.

mean square errors (MSEs) of channel estimation which is normalized to channel power for 16QAM modulation at the vehicle speed (ν_e) of 120 km/hr. The proposed two-stage channel estimation method has much lower MSE than the 2-D interpolation methods. Moreover, the curves of the 2-D interpolation methods present an error floor phenomenon. The 2-D interpolation methods with limited pilot information cannot recover the channel variations well in outdoor fast and selective fading channels. The MSEs of the proposed method and the 2-D interpolation method with cubic interpolation in frequency axis are about 3.7×10^{-3} and 2.6×10^{-2} at E_b/N_0 of 30 dB, respectively. The 2-D interpolation methods without transform processing have lower implementation complexity, but their performances are much inferior to our proposed method, especially in outdoor fading channels.

Fig. 16 shows the uncoded bit error rate (BER) performance under different vehicle speeds (ν_e) at E_b/N_0 of 16 dB. The Doppler frequency (f_D) is normalized to a subcarrier spacing. The result with the known perfect CSI is also included for benchmarking. At ν_e of 120 km/hr ($f_D = 0.025\Delta f$), the BERs of the perfect CSI, the floating- and fixed-point simulations of the proposed baseband receiver with four tracking iterations for QPSK/16QAM are $8.5 \times 10^{-4}/5.5 \times 10^{-3}$, $9.6 \times 10^{-4}/7.7 \times 10^{-3}$, and $9.9 \times 10^{-4}/8.1 \times 10^{-3}$, respectively. The performances of the proposed receiver with four and five tracking iterations have no obvious difference, so the process with four tracking iterations is enough to achieve an acceptable BER performance in high mobility environments. Even at ν_e of 240 km/hr ($f_D = 0.051\Delta f$), the BERs of the fixed-point simulation of the proposed receiver with four tracking iterations for QPSK/16QAM can achieve about $3.3 \times 10^{-3}/3.0 \times 10^{-2}$. Because the word lengths of each block are decided by the output SNR simulation, the floating- and fixed-point performances have shown that the implementation loss is very small. When operating at ν_e of 120 km/hr for QPSK/16QAM, the fixed-point performance has about 0.2/0.5 dB gap in E_b/N_0 as compared with the floating-point performance at $BER = 10^{-3}/10^{-2}$.

In AWGN channel, the performance requirement of IEEE 802.16e and that of our proposed receiver are shown in Table III. The channel coding uses the convolutional code specified by

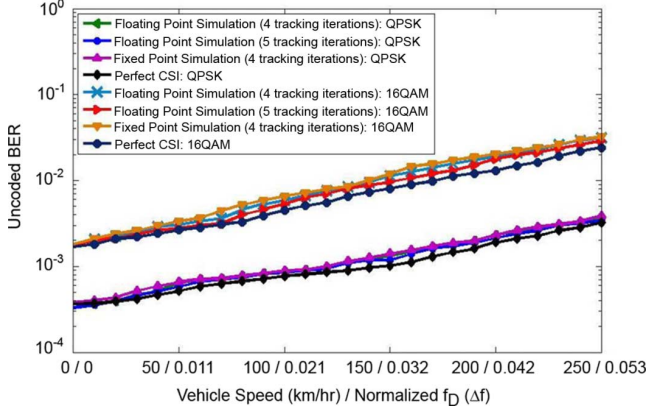


Fig. 16. Uncoded BER performance versus the vehicle speed.

TABLE III
REQUIRED SIGNAL-TO-NOISE RATIO FOR BER $< 10^{-6}$ IN AWGN CHANNEL

Modulation	QPSK		16QAM		64QAM		
Code Rate	1/2	3/4	1/2	3/4	1/2	2/3	3/4
Spec. of 802.16e (dB)	5.0	8.0	10.5	14.0	16.0	18.0	20.0
Proposed receiver (dB)	3.9	6.1	8.2	11.1	13.7	15.9	17.2

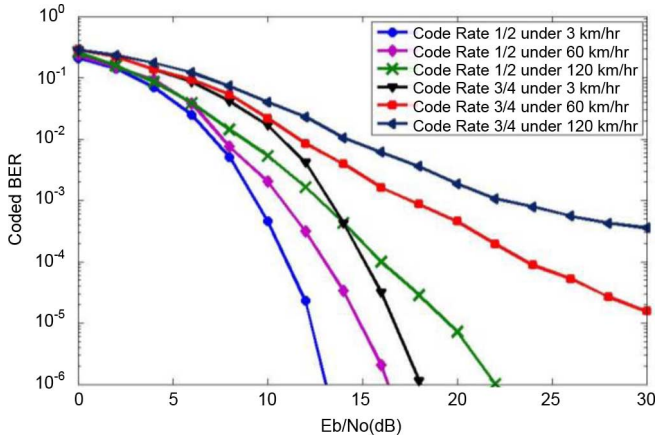


Fig. 17. Coded BER performance for 16QAM modulation.

IEEE 802.16e. It clearly shows that the proposed receiver meets the requirements of IEEE 802.16e in fixed environment. Fig. 17 shows the coded BER performance of the proposed receiver combining with the convolutional code for 16QAM modulation. IEEE 802.16e specification does not provide the performance requirement in mobile transmission. However, in code rate 1/2, the proposed receiver at v_e of 3, 60, and 120 km/hr can achieve the coded BER less than 10^{-6} with E_b/N_0 of 13.1, 16.1, and 22.1 dB. In code rate 3/4, the proposed receiver under 3 km/hr can achieve the coded BER less than 10^{-6} with E_b/N_0 of 18.2 dB. Even at v_e of 60 and 120 km/hr, the proposed receiver in code rate 3/4 can achieve the coded BER to about 10^{-5} and 10^{-4} . However, IEEE 802.16e standard provides the advanced channel coding schemes such as block turbo code (BTC), convolutional turbo code (CTC) and low density parity check code (LDPC) as the optional modes, and these schemes may further improve the coded BER performance [2].

TABLE IV
POST-LAYOUT RESULT OF THE PROPOSED RECEIVER

Technology	CMOS 90nm 1P9M, 1V	
Sampling Frequency	11.2 MHz	
Clock Frequency	78.4 MHz	
Size (mm ²)	Core	2.41×2.41
	Chip	3.21×3.21
Gate Count (gates)	1,386.5 K	
SRAM Size (bits)	412.5 K	
Power (mW)	68.48	

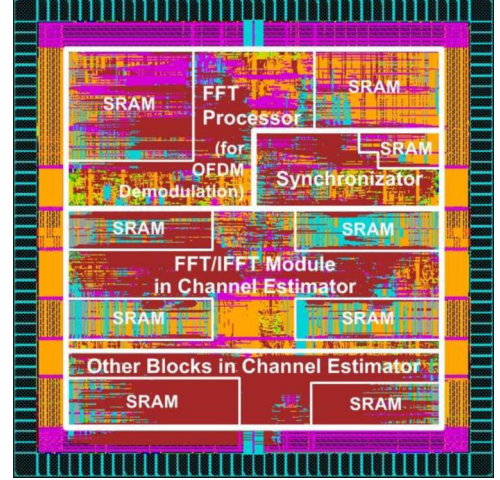


Fig. 18. Chip layout of the proposed STBC-OFDM downlink baseband receiver IC.

The proposed receiver is implemented in 90-nm 1P9M 1 V CMOS technology. The post-layout result of the proposed receiver is summarized in Table IV, and the chip layout is shown in Fig. 18. The gate count is about 1386.5 K gates. There are two clocks, 11.2 and 78.4 MHz, to be used as the sampling frequency and the operating frequency, respectively. The power is 68.48 mW. The uncoded throughput can support up to 27.32 Mbps for 16QAM modulation. The core size of this chip is 2.41×2.41 mm², and the chip size is 3.21×3.21 mm². The proposed system has two transmit antennas and one receive antenna, so the two channel responses of different antenna pairs must be estimated and STBC decoded with the two received OFDM symbols within a time slot. These process executions must satisfy that an OFDM symbol times is $102.9 \mu s$ as defined in Table I. An OFDM symbol time is dominated by the required execution cycles in the initialization stage. Therefore, the operating frequency of 78.4 MHz is determined by considering the power design issue and the standard requirements. However, based on this operating frequency, the proposed receiver can support up to four tracking iterations for the channel tracking. Table V shows the post-layout results of each block in the proposed receiver. The area proportions of the synchronizer, the FFT processor arranged with five memory banks, and the two-stage channel estimator are about 7.26%, 30.75%, and 61.99%. Because the IFFT/FFT module in the two-stage channel estimator must transform two CIRs or CFRs of different antenna pairs, it requires two computed kernels and four memory banks

TABLE V
POST-LAYOUT RESULTS OF EACH BLOCK IN THE PROPOSED RECEIVER

Module	Area (mm ²)	SRAM (bits)	Total Gates	Power (mW)
Synchronizer	0.402	20.5K	100.6K	0.307
FFT for OFDM Demodulation	1.707	196.8K	426.3K	14.42
Two-stage Channel Estimator	3.435	195.2K	859.6K	43.71
FFT/IFFT in the Channel Estimator	2.311	187.4K	578.4K	29.74

TABLE VI
HARDWARE SAVING BASED ON THE PROPOSED RECEIVER STRUCTURE

	This Work	Other Design Techniques
Delay Buffer	Single-Port Register File	Dual-Port SRAM [28]
	0.076 mm ² (2×512×20)	0.106 mm ² (1024×20)
Match Filter	Unsigned Calculation	Signed Calculation [28]
	0.109 mm ²	0.151 mm ²
Overall Synchronizer	Proposed	Direct Implementation
	0.402 mm ²	0.888 mm ²
One Memory Module in FFT/IFFT module	Single-Port Register File	Dual-Port SRAM [29]
	0.023 mm ² (128×46)	0.054 mm ² (128×46)
Two-stage Channel Estimator excluding FFT/IFFT module	Proposed	Direct Implementation
	1.124 mm ²	7.562 mm ²
Channel Estimation for One Antenna Pair	Proposed	Haene [30]
	422.6 K gates (90nm) 1024-point OFDM symbol	60.6 K gates (25μm) 64-point OFDM symbol

to support these calculations. The IFFT/FFT module occupies about 67.28% of the two-stage channel estimator.

Table VI lists the hardware saving based on the proposed receiver structure. The design techniques that are adopted in other OFDM receivers are evaluated to compare under the same function, system timing requirement, and 90-nm CMOS technology. The delay buffers for the synchronizer and one memory module with the size of 128 × 46 bits for the FFT/IFFT module using single-port register file modules can save about 28% to 57% area than that use dual-port SRAM modules. However, a single-port register file module just can support one read or write in a clock cycle, so it may require more access cycles than a dual-port SRAM module for data reading and writing. In the proposed receiver design, we relax the access time constrain and well arrange the data process and memory access schedule, so we can use low-cost single-port register file modules without access conflict. The proposed match filter only uses NAND and NOR gates to perform the unsigned calculation and saves about 28% area than that adopts signed calculation. The overall synchronizer design can reduce about 55% area as compared with the design adopting signed calculation and dual-port SRAM modules. Moreover, by using our proposed scheme and architecture, the two-stage channel estimator excluding FFT/IFFT module improves 85.2% of that is directly implemented. Finally, we provide a comparison with a similar channel estimator work [30] implemented by a transform domain ML method. Since the two designs have distinct functions and implemented in different technology, a fair comparison between them is hard to carry out. When the operating frequency is set to 200 MHz as same as the work [30], the proposed channel estimator requires about 422.6 K gates for one pair channel estimation without STBC decoding. If a design efficiency gain is defined as the OFDM symbol size

TABLE VII
BASEBAND RECEIVER DESIGNS FOR WMAN

	Chang [31]	Chuang [32]	This Work
Technology	0.18μm	90nm	90nm
OFDM Symbol Size	256 points	1024 points	1024 points
System Architecture	SISO	1×2 SIMO	2×1 MISO
Sampling / Operating Frequency (MHz)	6.8 / 30.0	11.2 / 50.0	11.2 / 78.4
Area Size (mm ²)	1.70×1.71	About 1/3 of 6.96×7.01	2.41×2.41
Gate Count (gates)	0.22 M	3.33 M	1.38 M
Power (mW)	113.81	600 (whole transceiver chip)	68.48

normalized by the design gate count, our work can get the efficiency gain 2.29 times of the work [30].

Table VII lists the comparisons of our proposed receiver design with the similar works for WMAN [31], [32]. The work [31] proposed a single-input single-output (SISO) 256-point OFDM receiver for fixed WMAN. The work [32] proposed a 1 × 2 single-input multiple-output (SIMO) 1024-point OFDM baseband transceiver for mobile WMAN. The work [32] did not provide the proportion of the inner receiver design, but the inner receiver occupied about 1/3 of the whole chip as seen from the chip photo. These two works adopted the interpolation-based channel estimator. Since the works have different technology and different OFDM system architecture, the fair comparisons between them are hard to carry out. Although our design gate count is 6.27 times of the work [31], our design can support 1024-point OFDM symbol processing that is 4 times of the symbol size of the work [31], and it can simultaneously estimate and STBC decode the received data transmitted from two different antennas. The sampling frequency of our design is 1.65 times of that of the work [31]. Moreover, the work [31] just proposed for fixed WMAN. As compared with the work [32], the area of the work [32] is about 2.8 times of our proposed design, but these two designs are applied to 1 × 2 SIMO and 2 × 1 multiple-input single-output (MISO) STBC-OFDM systems. The 1 × 2 STBC-OFDM system requires paying more design effort on the receiver side, but the some computation blocks can be shared. Therefore, the design requirement of the 1 × 2 STBC-OFDM receiver shall be less than 2 times of that of the 2 × 1 STBC-OFDM receiver.

In summary, we propose a STBC-OFDM downlink baseband receiver for mobile WMAN. The proposed receiver effectively improves the design complexity with acceptable hardware cost while keeping the high performance in multipath fading channels.

VI. CONCLUSION

In this paper, we propose a downlink baseband receiver for mobile WMAN that is applied in the STBC-OFDM system with two transmit antennas and one receive antenna. A simple symbol boundary detector, a carrier frequency recovery loop modified by the ping-pong algorithm, and an accurate two-stage channel estimator are effectively implemented. Although the two-stage channel estimator requires higher hardware cost as compared with the interpolation-based channel estimators, it has significant performance improvement for successfully

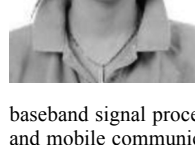
realizing the STBC-OFDM system in outdoor mobile environments. From the simulation results, we have shown that the proposed receiver improves about 8.5 dB of the normalized MSE for 16QAM modulation as compared with that adopting the 2-D interpolation methods in multipath fading channels. Moreover, under the vehicle speed of 120 km/hr, the convolutional coded BER for 16QAM modulation can achieve less than 10^{-6} with coded rate of 1/2. The proposed receiver designed in 90-nm CMOS technology can support up to 27.32 Mbps (uncoded) downlink throughput under 10 MHz channel bandwidth. This design has a core area of $2.41 \times 2.41 \text{ mm}^2$ and dissipates 68.48 mW at 78.4 MHz operating frequency. With verifications through all of the simulations and design results, the proposed baseband receiver can provide a solid foundation for WMAN in fixed and mobile wireless communication.

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