

行政院國家科學委員會補助專題研究計畫 ☐期中進度報告

☒期末報告

奈米互補式金氧半場效電晶體靜態隨機存取記憶體靜態雜訊邊界與

負偏壓溫度效應/正偏壓溫度效應之量測與特性化電路結構設計

計畫類別：☒個別型計畫 ☐整合型計畫

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中 華 民 國 101 年 10 月 30 日

電子工程學系

計畫名稱：奈米互補式金氧半場效電晶體靜態隨機存取記憶體靜態雜訊邊界與負偏壓溫度效應/正偏壓溫度效應之量測與特性化電路結構設計

研究者：莊景德，周世傑

經費來源：行政院國家科學委員會

關鍵詞：靜態隨機存取記憶體穩定度；靜態雜訊邊界；長時間可靠度劣化；負偏壓溫度效應；正偏壓溫度效應

隨著製程微縮至次-100 奈米領域，漏電、元件參數變異、及長時間可靠度劣化已成為互補式金氧半場效電晶體靜態隨機存取記憶體的穩定度、可微縮性、及效能的主要限制。先進微處理機所使用的快速記憶體及系統晶片(SoC) 的嵌入式記憶體需要大容積的靜態隨機存取記憶體及超過 ± 5 個標準差 (5σ) 的設計規格。因此以儲存位元及/或靜態隨機存取記憶體產品層次的位元列陣為基礎來設計的特定量測與特性化電路結構設計日益重要。與此同時，金氧半場效電晶體靜態隨機存取記憶體的生命週期可靠度由於受到各種長時間可靠度劣化現象，如熱載子效應 (Hot Carrier Effect)、P-型場效電晶體的負偏壓溫度效應、高電介質金屬閘極 N-型場效電晶體的正偏壓溫度效應、時間相依介電質崩潰、輻射性損壞等，的影響而急遽惡化。其中負偏壓溫度效應與正偏壓溫度效應使得臨界電壓， V_T ，隨著使用的生命週期而偏移。因此之故，用以量測負偏壓溫度效應及正偏壓溫度效應，並能讓設計者施以適當的劣化加速壓溫以量測及特性化其對記憶體穩定度劣化影響的量測電路結構已成為一個重要的研發課題。

在這個 2 年的研究計劃中，我們將與智原科技，針對奈米級靜態隨機存取記憶體的靜態雜訊邊界及負偏壓溫度效應與正偏壓溫度效應，共同研發量測與特性化的電路結構。我們將併行研發以儲存位元為基礎 (如環型振盪器) 及以靜態隨機存取記憶體產品層次的位元列陣 (SRAM cell array) 為基礎的特定量測與特性化電路結構及量測技術。更進一步地，我們會將研發的電路結構及量測技術應用到靜態隨機存取記憶體的穩定度及複晶閘極 (poly-gate) 互補式金氧半場效電晶體靜態隨機存取記憶體的負偏壓溫度效應的量測及特性化。我們更將建構一套陣列層級讀取及寫入監/量測技術用以量測靜態隨機存取記憶體位元陣列的雜訊邊界特性，藉此架構使得電路設計者可以得到關於靜態隨機存取記憶體穩定度更多有意義的相關設計資訊。最後，我們將會建構一套可以整合觀察負溫度偏壓效應/正溫度偏壓效應造成的退化效應與靜態隨機存取記憶體穩定度的架構。

Department of Electronics Engineering

Title : Measurement and Characterization Structures for Static Noise Margin and NBTI/PBTI Degradation of Nanoscale CMOS SRAM

Principal Investigator : Ching-Te Chuang and Shyh-Jye Jou

Sponsor : National Science Council

Keywords : SRAM Stability, Static Noise Margin, Long Term Degradation, Negative Bias Temperature Instability, Positive Bias Temperature Instability

With technology scaling down to deep sub-100 nm regime, leakage, variation and long-term degradation have surfaced to constrain the stability, scalability and attainable performance of CMOS SRAM. State-of-the-art processor cache memory and SoC embedded memory require large capacity SRAM with over $\pm 5\sigma$ design, and the ability to measure/characterize the Static Noise Margin (SNM) based on specific cell test structures and/or product level SRAM array has become ever-increasingly important. Meanwhile, the lifetime reliability of nanoscale CMOS SRAM suffers from long term degradation such as Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI, for pMOS), Poasitive Bias Temperature Instability (PBTI, for high- κ metal-gate nMOS), Time-Dependent Dielectric Breakdown (TDDB), radiation-induced damage, etc.. In particular, NBTI/PBTI cause the threshold voltage, V_T , to drift over the life span of usage, thus severely degrading the stability, margin, performance, and lifetime reliability. As such, SRAM NBTI/PBTI measurement structures, which allow designers to apply relevant stresses and characterize resulting stability degradation, have become a key research subject.

In this 2 year project, jointly with Faraday Technology Corporation (智原科技), we will develop measurement and characterization structures for Static Noise Margin and NBTI/PBTI for nanoscale CMOS SRAM. Both individual cell based structures (e.g. ring oscillator) and product array level techniques will be investigated. We will then apply the structures and measuring techniques to the characterization of SRAM stability and NBTI degradation (for poly-gate technology). Further, we will develop array-level measurement techniques to observe the characteristics of cells in SRAM cell array, and develop the architecture for measuring the Static Noise Margin (SNM) to provide designer with more direct and significant information about the SRAM stability and design margin. Finally, we will build up a bridge between the measurement of NBTI and PBTI degradation and the resulting impact on SRAM

With technology scaling down to deep sub-100 nm regime, leakage, variation and long-term degradation have surfaced to constrain the stability, scalability and attainable performance of CMOS SRAM [1]. The rapid increase in local random V_T variation, against the backdrop of lower supply voltage and increasing memory capacity in state-of-the-art processors and SoC, has rendered the redundancy needed for repair impractical, and even prohibitive for designs below $\pm 5\sigma$. For 6T SRAM, the major limiting factors in the design domain are the conflicting Read/Write requirements and cell disturbs [1, 2]. The variations in the Read-disturb voltage (“Cell down-level”) and inverter Trip voltage (“Cell switch-point”) increase, causing overlap and thus failure starting at 90 nm node [2]. As such, the ability to physically measure/characterize the SRAM Static Noise Margin (SNM) [3] has become increasingly important for proper understanding, modeling, and calibration of the design margin to ensure acceptable yield under the target performance metrics.

In addition to leakage and variation, NBTI (Negative Bias Temperature Instability) [4] has long been a limiting factor in the scaling of PMOS. At high negative bias and elevated temperature, the PMOS V_T gradually drifts to become more negative, thus reducing PMOS current drive and affecting cell stability, margin, and V_{MIN} of SRAM [5]. Furthermore, with high- κ gate materials, PBTI (Positive Bias Temperature Instability) in NMOS must be considered, as high- κ gates exhibit significant charge trapping and thus V_T shift in NMOS [6].

These long term V_T drift and other gate oxide related V_T degradation mechanisms must be properly accounted for over the SRAM life span of usage [7-9]. Hence, SRAM stability and NBTI/PBTI measurement/characterization structures, which allow designers to apply relevant stresses and characterize stability and degradation, have become a key research subject.

The measurement/characterization structures for Static Noise Margin and NBTI/PBTI degradation can be either individual cell/device based or in a product array level environment. The individual cell based Static Noise Margin measurement/characterization structures are typically used in the early stage of SRAM cell technology/process development, where developers need to characterize various cell design/layout/groundrules, and through hardware cycles and measurement/characterization, decide on the final/proper cells to use. Typical structures consists of column or columns of cells with all internal nodes of a cell accessible externally [10, 11].

For measurement/characterization of NBTI/PBTI for individual devices, the most primitive approach utilizes two simple standard ring oscillators. One of the ring oscillators goes through NBTI/PBTI stress, and the frequency of this “stressed” ring oscillator is then compared with that of the “unstressed” ring oscillator. The resulting frequency difference gives an indication of the NBTI/PBTI degradation of the devices in the “stressed” ring oscillator. To enhance the sensitivity of the ring oscillator based structures, various techniques based on “Beat Frequency” difference of two ring oscillators have been developed, where a phase

difference between the two ring oscillators is introduced by tapping logic [12] or a phase shifter [13]. As the “Beat Frequency” depends on the signal edge alignment of the two ring oscillators, a small drift of the frequency (hence the signal phase) of the “stressed” ring oscillator results in a large change in the “Beat Frequency”, thus significantly enhancing the sensitivity. To separate the NBTI and PBTI effects, improved “Cut-and-Bias” ring oscillator circuit with the flexibility of isolated or combined NBTI and PBTI measurement has been developed [14].

While individual cell/device based characterization structures can offer detail characteristics of the individual subjects, it is preferable and essential to characterize the Static Noise Margin and NBTI/PBTI degradation in product array like environment so as to capture all the lithography and process related effects. To accurately characterize the unstressed and stressed SRAM devices, it is necessary to place the devices as densely packed as they are in the normal SRAM array. It is also important that the layout around the measured device is as close as possible to the layout of the original SRAM array to incorporate all the effects of the dense layout and the applied ground rule waivers not present in isolated single transistors [15]. This kind of scheme allows gathering of data of important cell device characteristics in a “real” “product-like” environment.

With modified SRAM column architecture which allows external access to individual bit-line and/or word-line, one can gather information on Read Static Noise Margin (RSNM) and Write Margin (WM) by measuring bit-line current under various voltage sweep [16, 17, 18]. This kind of scheme maintains the SRAM cell layout in “real” product, with changes only in the peripheral logic to allow external access to Word-Line (WL) and Bit-Line for voltage sweep and current measurement.

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研究目的。

In this 2 year project, jointly with Faraday Technology Corporation (智原科技), we intend to develop measurement and characterization structures for Static Noise Margin (SNM) and NBTI/PBTI for nanoscale CMOS SRAM, and apply the structures and techniques to the characterization of SRAM stability and NBTI degradation (for poly-gate technology).

研究方法。

Both individual cell based structures (e.g. ring oscillator) and product array level techniques have been

investigated. Individual cell based structure has been developed based UMC's 55nm 6T SRAM cell. The array-level measurement techniques have been developed based on SRAM macros relevant to Faraday's (智原科技) 55nm SRAM compilers.

The developed individual cell based structures and product array level techniques have been validated by extensive simulations. Test sites and Test SRAM macros with reasonable/meaningful size (determined based on discussion with Faraday) have been designed. Based on the obtained hardware, we will carry out measurement/characterization, and analyze the data to understand the characteristic of Static Noise Margin and NBTI/PBTI degradation on SRAM. We will also try to correlate the measured data with simulation results.

We also collaborated with our former colleagues at IBM T. J. Watson Research Center to engage High- κ Metal-Gate Group and SRAM and Technology-Circuit Co-Design members in VLSI Design Department, and Georgia Tech., to develop Ring Oscillator Monitoring Structures for isolated/combined NBTI and PBTI Measurement. The monitoring structures have been implemented, and measurement/characterization have been carried out in both SiO₂/poly-gate technology and high-k metal-gate technology.

We further collaborated with our former colleagues at IBM T. J. Watson Research Center and University of Utah, Salt Lake City, UT, U.S.A. to develop a Slew-Rate Monitoring circuit for on-chip process variation detection. The Slew-Rate Monitor has been fabricated and characterized in 65 nm IBM CMOS technology.

全程結果與討論。

1. Embedded SRAM Ring Oscillator for In-Situ Measurement of NBTI and PBTI Degradation in CMOS 6T SRAM Array

We have developed a novel embedded SRAM ring oscillator structure and measurement technique to characterize the BTI degradation of 6T SRAM cell transistors in a real SRAM cell array environment. The embedded ring oscillators are built using the 6T SRAM cell transistors directly in a real SRAM cell array environment, thus providing direct correlation between measured BTI degradation of cell transistors and the resulting impacts on SRAM stability. The viability of the embedded ring oscillator odometer and the impact of bias temperature instability have been implemented/demonstrated in UMC 55nm Standard Performance (SP) CMOS technology. Measurement and characterization have been carried out, and the results have been presented in a conference paper at 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT):

Ming-Chien Tsai, Yi-Wei Lin, Hao-I Yang, Ming-Hsien Tu, Wei-Chiang Shih, Nan-Chun Lien, Kunti Lee, Shyh-Jye Jou, Ching-Te Chuang, and Wei Hwang, "Embedded SRAM Ring Oscillator for In-Situ Measurement of NBTI and PBTI Degradation in CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, April

23-25, 2012.

This paper is attached in the Appendix (附錄).

A patent application for this “Embedded 6T SRAM Ring Oscillator for NBTI/PBTI Measurement” is being applied by 世界專利商標事務所。

莊景德, 周世傑, 黃威, 蔡銘謙, 林宜緯, 楊皓義, 杜明賢, 石維強, 連南鈞, 李坤地, “用以量測負偏壓溫度效應/正偏壓溫度效應之內嵌式 6T 靜態隨機存取記憶體環形振盪器” (Embedded 6T SRAM Ring Oscillator for NBTI/PBTI Measurement)。11(專)A040, 中華民國及美國專利由世界專利商標事務所申請中。(國立交通大學)。

2. An Array Based All-Digital On-Chip Circuit for 6T SRAM Stability Measurement

We have developed an array based test structure to measure the noise margin of standard 6T SRAM. In this work, the Read Static Noise Margin (RSNM) is characterized by separating the Read Disturb Voltage (V_{read}) and Inverter Trip Voltage (V_{trip}). The 6T SRAM cell is modified to allow direct read-out of the Read Disturb Voltage and Inverter Trip Voltage from the SRAM Array. We modify only the metal layers over the cell while keeping the diffusion, poly and contact layers intact, so as to maintain the thin cell layout with horizontal uni-directional poly, and pattern density/symmetry. Acquired voltage data are measured by all digital measurement circuit scheme composed of VCO and counter with resolution of 0.167mV/bit. Write Margin (WM) is measured by stepping down the BL voltage until the Write operation fails. The scheme has been implemented in a 512Kb SRAM array in UMC 55nm Standard Performance (SP) technology, and the results have been presented in a conference paper at 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT):

Yi-Wei Lin, Ming-Chien Tsai, Hao-I Yang, Geng-Cing Lin, Shao-Cheng Wang, Ching-Te Chuang, Shyh-Jye Jou, Wei Hwang, Nan-Chun Lien, Kuen-Di Lee and Wei-Chiang Shih, “An All-Digital Read Stability and Write Margin Characterization Scheme for CMOS 6T SRAM Array,” Proc. 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, April 23-25, 2012.

This paper is attached in the Appendix (附錄).

A patent application for this “Array Based All-Digital On-Chip V_{trip} , V_{read} , and WM Measurement Circuit for 6T SRAM” is being applied by 世界專利商標事務所。

莊景德, 周世傑, 黃威, 林宜緯, 蔡銘謙, 楊皓義, 杜明賢, 石維強, 連南鈞, 李坤地, “6T 靜態隨機存取記憶體陣列之量測轉態電壓、讀取干擾與寫入邊界的方法與架構” (Methods and Apparatus for Measuring V_{trip} , V_{read} , and WM of 6T SRAM Array)。中華民國及美國專利由世界專利商標事務所申請中。

3. An All-Digital Bit Transistor Characterization Scheme for CMOS 6T SRAM Array

We have developed an all-digital bit transistor characterization scheme for CMOS 6T SRAM array. The scheme employs an on-chip operational amplifier feedback loop to measure the individual threshold voltage (V_{TH}) of 6T SRAM bit cell transistors (holding PMOS, pull-down NMOS, and access NMOS) in SRAM cell array environment. The measured voltage is converted to frequency with dual VCO and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. A 512Kb test chip is implemented in 55nm 1P10M Standard Performance (SP) CMOS technology. Monte Carlo simulations indicate that the accuracy of the V_{TH} measurement scheme is about 2-7mV at TT corner across temperature range from 85°C to -45°C, and post-layout simulations show the resolution of the digital read-out scheme is < 0.2mV per bit. Measured V_{TH} distributions agree well with Monte Carlo simulation results. The results have been presented in a conference paper at 2012 IEEE International Symposium on Circuits and Systems (ISCAS).

Geng-Cing Lin, Shao-Cheng Wang, Yi-Wei Lin, Ming-Chien Tsai, Ching-Te Chuang, Shyh-Jye Jou, Nan-Chun Lien, Wei-Chiang Shih, Kuen-Di Lee, and Jyun-Kai Chu, "An All-Digital Bit Transistor Characterization Scheme for CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, May 20-23, 2012, pp. 2485-2488.

This paper is attached in the Appendix (附錄).

A patent application for this "Array Based All-Digital Threshold Voltage Measurement Scheme for 6T SRAM" is being applied by 世界專利商標事務所。

莊景德、周世傑、林耕慶、王紹丞、林宜緯、蔡銘謙、石維強、連南鈞、李坤地、朱俊愷，"臨界電壓量測裝置(Threshold Voltage Measurement Device)" Y/R:11(專)A167US, 中華民國及美國專利由世界專利商標事務所申請中。(國立交通大學)。

4. Reliability Monitoring Ring Oscillator Structures for Isolated/Combined NBTI and PBTI Measurement in High-K Metal Gate Technologies

Together with our former colleagues in the High- κ Metal-Gate Group and SRAM and Technology-Circuit Co-Design members in VLSI Design Department at IBM T. J. Watson Research Center, and Georgia Tech., we have developed Ring Oscillator Monitoring Structures for isolated/combined NBTI and PBTI Measurement. The monitoring structures have been implemented in high-k metal-gate technology. The measurement results clearly show significant RO frequency degradation from PBTI as well as NBTI. For comparison, RO structures with the same principle are also implemented in a SiO₂/poly-gate technology, where PBTI is negligible. Experimental results show noticeable frequency degradation under NBTI-only stress mode but negligible degradation under PBTI-only mode, which illustrates the validity of the proposed principle and structures. The results have

Lake City, UT, U.S.A., we have developed a Slew-Rate Monitoring circuit for on-chip process variation detection. The difference of rise and fall slew is presented as another process-variation metric along with the delay in determining the relative mismatch between the drive strengths of nMOS and pMOS devices. The importance of considering both of these metrics is illustrated, and a new slew rate monitoring circuit is presented for measuring the difference of rise and fall slew of a signal on the critical path of a circuit. Sensitivity analysis with multiple pulses as input has also been investigated. Bias generator circuits that track nMOS and pMOS threshold voltages have been incorporated, which makes the design less susceptible to process variation. Design considerations, simulation results, and characteristics of the slew-rate monitor circuitry in a 65-nm IBM CMOS process are presented, and a sensitivity of 50 MHz/50 ps for single pulse input is achieved. The measurement sensitivity of a fabricated slew-rate monitor in a 65-nm IBM CMOS technology is 0.11 V/ μ s, with 1089 pF as the output load of the slew-rate monitor. The results are presented in a paper to appear in IEEE Transactions on Very Large Scale Integration Systems (TVLSI).

Amlan Ghosh, Rahul M. Rao, Jae-joon Kim, Ching-Te Chuang and Richard B. Brown, “Slew-Rate Monitoring Circuit for On-Chip Process Variation Detection,” IEEE Transactions on Very Large Scale Integration Systems (TVLSI), (accepted).

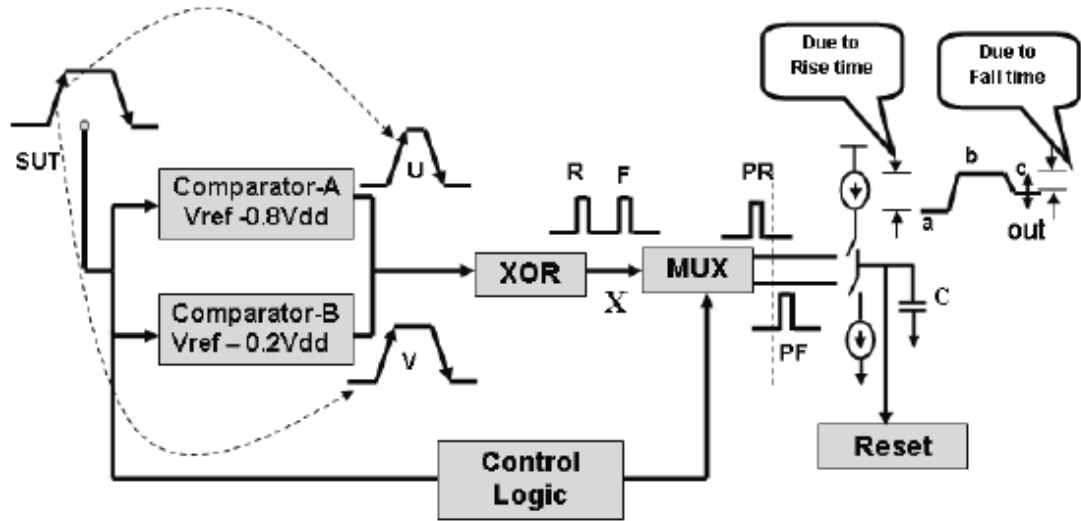


Fig. 3. Block diagram of the slew-rate monitor.

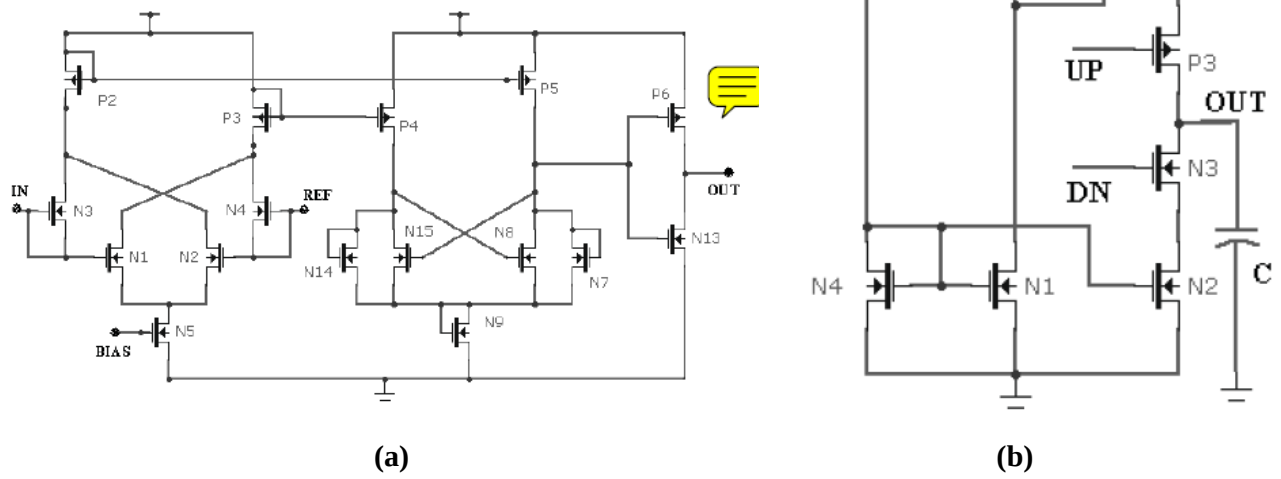


Fig. 4. Schematic block diagram of (a) comparator-A, and (b) integrator.

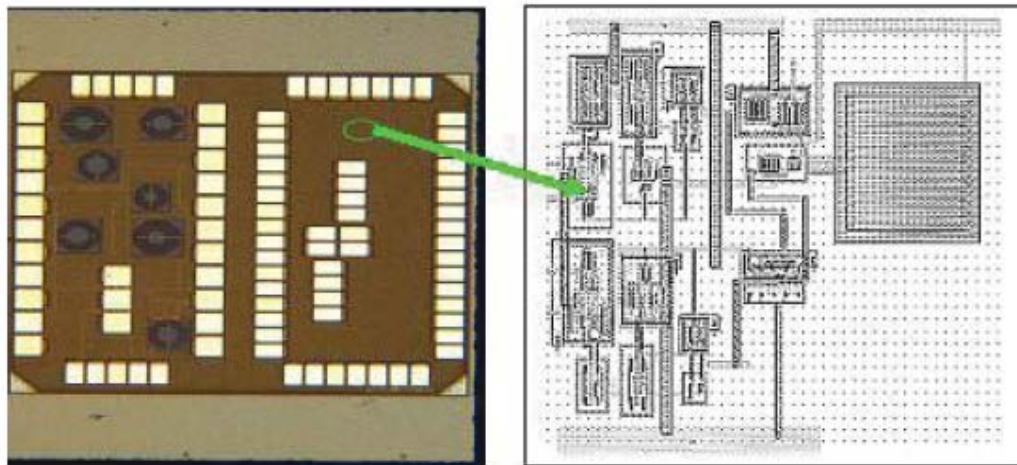


Fig. 5. Chip micrograph and physical layout of the slew-rate monitoring circuit.

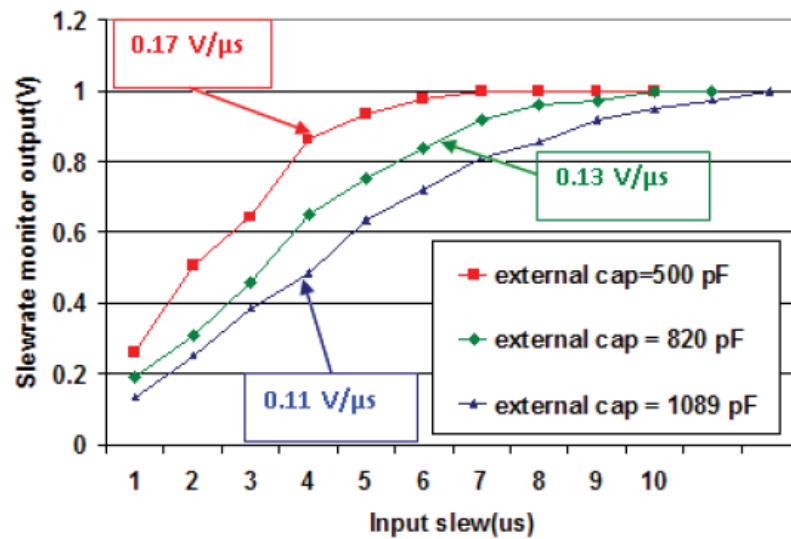


Fig. 6. Measured sensitivity of the slew-rate monitoring circuit.

全程計劃產出論文及專利表列。

(A) 4 Conferen Papers:

1. Ming-Chien Tsai, Yi-Wei Lin, Hao-I Yang, Ming-Hsien Tu, Wei-Chiang Shih, Nan-Chun Lien, Kunti Lee, Shyh-Jye Jou, Ching-Te Chuang, and Wei Hwang, "Embedded SRAM Ring Oscillator for In-Situ Measurement of NBTI and PBTI Degradation in CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, April 23-25, 2012.
2. Yi-Wei Lin, Ming-Chien Tsai, Hao-I Yang, Geng-Cing Lin, Shao-Cheng Wang, Ching-Te Chuang, Shyh-Jye Jou, Wei Hwang, Nan-Chun Lien, Kuen-Di Lee and Wei-Chiang Shih, "An All-Digital Read Stability and Write Margin Characterization Scheme for CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, April 23-25, 2012.
3. Geng-Cing Lin, Shao-Cheng Wang, Yi-Wei Lin, Ming-Chien Tsai, Ching-Te Chuang, Shyh-Jye Jou, Nan-Chun Lien, Wei-Chiang Shih, Kuen-Di Lee, and Jyun-Kai Chu, "An All-Digital Bit Transistor Characterization Scheme for CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, May 20-23, 2012, pp. 2485-2488.
4. Jae-Joon Kim, Barry P. Linder, Rahul M. Rao, Tae-Hyoung Kim, Pong-Fei Lu, Keith A Jenkins, Chris H. Kim, Aditya Bansal, Saibal Mukhopadhyay, and Ching-Te Chuang, "Reliability Monitoring Ring Oscillator Structures for Isolated/Combined NBTI and PBTI Measurement in High-K Metal Gate Technologies," Proc. 2011 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, April 10-14, 2011, pp. 47-50.

(B) 1 Journal Paper:

1. Amlan Ghosh, Rahul M. Rao, Jae-joon Kim, Ching-Te Chuang and Richard B. Brown, "Slew-Rate Monitoring Circuit for On-Chip Process Variation Detection," IEEE Transactions on Very Large Scale Integration Systems (TVLSI), (accepted).

(C) 3 Patents:

1. 莊景德, 周世傑, 黃威, 蔡銘謙, 林宜緯, 楊皓義, 杜明賢, 石維強, 連南鈞, 李坤地, "用以量測負偏壓溫度效應/正偏壓溫度效應之內嵌式 6T 靜態隨機存取記憶體環形振盪器" (Embedded 6T SRAM Ring Oscillator for NBTI/PBTI Measurement)。11(專)A040, 中華民國及美國專利由世界專利商標事務所準備申請中。(國立交通大學)。
2. 莊景德, 周世傑, 黃威, 林宜緯, 蔡銘謙, 楊皓義, 杜明賢, 石維強, 連南鈞, 李坤地, "6T 靜態隨機存取記憶體陣列之量測轉態電壓、讀取干擾與寫入邊界的方法與架構" (Methods and Apparatus for Measuring V_{trip} , V_{read} , and WM of 6T SRAM Array)。中華民國及美國專利由世界專利商標事務所準備申請中。(國立交通大學)。
3. 莊景德、周世傑、林耕慶、王紹丞、林宜緯、蔡銘謙、石維強、連南鈞、李坤地、朱俊愷, "臨界電壓量測裝置(Threshold Voltage Measurement Device)" Y/R:11(專)A167US, 中華民國及美國專利由世界專利商標事務所準備申請中。(國立交通大學)。

附錄。

1. Ming-Chien Tsai, Yi-Wei Lin, Hao-I Yang, Ming-Hsien Tu, Wei-Chiang Shih, Nan-Chun Lien, Kunti Lee, Shyh-Jye Jou, Ching-Te Chuang, and Wei Hwang, "Embedded SRAM Ring Oscillator for In-Situ Measurement of NBTI and PBTI Degradation in CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, April 23-25, 2012.
2. Yi-Wei Lin, Ming-Chien Tsai, Hao-I Yang, Geng-Cing Lin, Shao-Cheng Wang, Ching-Te Chuang, Shyh-Jye Jou, Wei Hwang, Nan-Chun Lien, Kuen-Di Lee and Wei-Chiang Shih, "An All-Digital Read Stability and Write Margin Characterization Scheme for CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, Taiwan, April 23-25, 2012.
3. Geng-Cing Lin, Shao-Cheng Wang, Yi-Wei Lin, Ming-Chien Tsai, Ching-Te Chuang, Shyh-Jye Jou, Nan-Chun Lien, Wei-Chiang Shih, Kuen-Di Lee, and Jyun-Kai Chu, "An All-Digital Bit Transistor Characterization Scheme for CMOS 6T SRAM Array," Proc. 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, May 20-23, 2012, pp. 2485-2488.

Embedded SRAM Ring Oscillator for In-Situ Measurement of NBTI and PBTI Degradation in CMOS 6T SRAM Array

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Abstract—One of the major reliability concerns in nano-scale CMOS VLSI design is the time-dependent Bias Temperature Instability (BTI) degradation. Negative Bias Temperature Instability and Positive Bias Temperature Instability (NBTI and PBTI) weaken MOSFETs over usage/stress time. We present an embedded 6T SRAM ring oscillator structure which provides in-situ measurement/characterization capability of cell transistor degradation induced by bias temperature instability. The viability of the embedded ring oscillator odometer and the impact of bias temperature instability are demonstrated in 55nm standard performance CMOS technology.

I. INTRODUCTION

Lifetime reliability is one of the key design factors for robust VLSI systems. Bias Temperature Instability (BTI), Hot Carrier Injection (HCI), and Time Dependent Dielectric Breakdown (TDDB) have become major concerns for performance and yield of nano-scale CMOS VLSI systems. These reliability degradations not only constrain the technology scaling, but also threaten the stability and functionality of digital circuits [1-4]. The degradation of device threshold voltage under the presence of electrical and thermal stress has long been a significant reliability issue in scaled CMOS technologies. Due to the importance of long-term degradation in nano-scale CMOS SRAM, there have been significant amount of efforts investigating the impacts of NBTI and PBTI on SRAM static/dynamic noise margins and cell failure probability [1, 2]. Kang et al. [2] explored the impact of NBTI degradation of several critical performance parameters of SRAM arrays. They showed that, under NBTI stress, the Static Noise Margin (SNM), READ stability, and parametric yield of SRAM array were severely degraded over time. On the other hand, Write-ability and leakage current might improve with time. Bansal et al. [3] carried out failure analysis using Monte-Carlo simulations and showed that, under worst-case static stress, NBTI and PBTI degraded the stability during READ (significantly) and WRITE (marginally) operations.

Ring Oscillator (RO) based structure for measuring NBTI degradation is the simplest method [5]. It has been shown that the relative degradation of NBTI stressed ring oscillator increases as the operating voltage decreases. Some on-chip reliability monitors for measuring degradation of digital circuits have been proposed [5-7]. The circuits in [5] overcome the drawbacks of conventional ring oscillators which fail to isolate the NBTI and PBTI contribution when PBTI isn't negligible anymore in deeply-scaled CMOS technology with

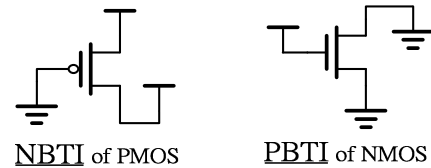


Fig. 1. NBTI stress of PMOS and PBTI stress of NMOS.

high- κ /metal-gate [8, 9]. Kim et al. [6] developed a silicon odometer with high sensing resolution by measuring the beat frequency of two ring oscillators. Furthermore, a monitoring structure [7], which can measure the frequency degradation induced by HCI, BTI, and TDDB separately, has been introduced for accurate real-time reliability monitoring. However, all of these monitoring structures were implemented in logic circuits with individual isolated logic devices to characterize the BTI effects on general digital logic devices/circuits, not for specific SRAM cell transistors in a real SRAM cell array environment.

In this work, we propose an embedded SRAM ring oscillator structure and measurement technique to characterize the BTI degradation of 6T SRAM cell transistors in a real SRAM cell array environment. The embedded ring oscillators are built using the 6T SRAM cell transistors directly in a real SRAM cell array environment, thus providing direct correlation between measured BTI degradation of cell transistors and the resulting impacts on SRAM stability. The details of the Embedded SRAM Ring Oscillator (ESRO) are presented in Section II. The analysis and measurement results are shown in Section III, and the conclusions of the paper are given in Section IV.

II. EMBEDDED SRAM RING OSCILLATOR

A. Embedded SRAM Ring Oscillator and BTI Stress

Fig. 1 shows a PMOS (NMOS) under NBTI (PBTI) stress, As mentioned above, the SRAM stability degradation induced by BTI significantly impacts the long-term reliability. As such, it is crucial to have a characterization structure that can provide direct measurement of cell transistor degradation due to aging effects. We modify the SRAM cell array to form an ESRO for BTI measurement. We combine the BTI stress capability and ring oscillator into ESRO structure. In 6T SRAM cell (Fig. 2), we are mainly concerned about the degradation of pull-up PMOS (NBTI) and pull-down NMOS (PBTI). The degradation of these two devices can affect the cell stability and performance significantly. For the access pass-gate transistor, the active period for a particular WL is typically relatively short during the whole SRAM operation.

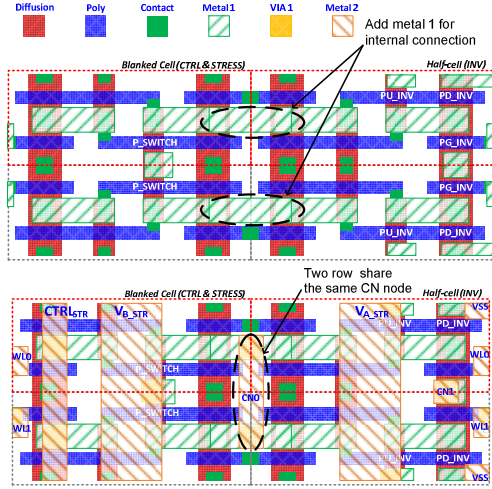


Fig. 5. Modification of 6T cell layout to form ESRO unit-stage.

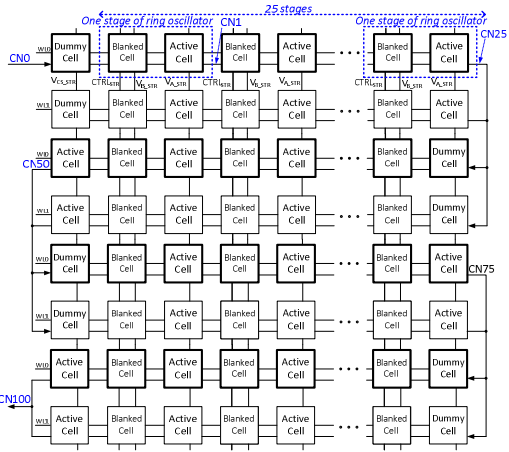


Fig. 6. 100-stage ESRO chain composed of modified SRAM cells.

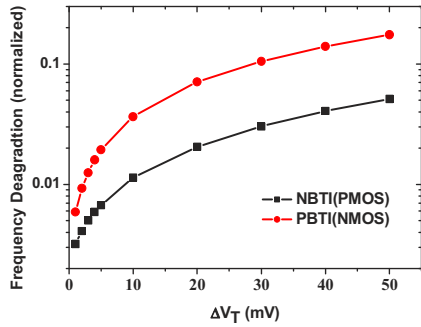


Fig. 7. Simulated frequency degradation vs. threshold voltage drift.

near the ring oscillator array. The dummy cells (CNn (n=0, 25, 50, 75)) used in 100-stage ring array are for passing signals and to preserve the SRAM cell array layout characteristics in each stage of ESRO. The delay time of entire ESRO is 34.5ns. Fig. 7 shows the simulated results of frequency degradation versus threshold voltage drift using modified cell device models. Based on 55nm 1P9M 1.0V SiO₂/poly-gate standard performance CMOS process, the oscillation frequency of ESRO is 14.5 MHz and the area of the two parallel 100 stages ESROs is 546.7 μm² (66.67μm*8.2μm), including the dummy

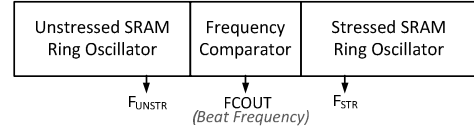


Fig. 8. One set of testing circuits

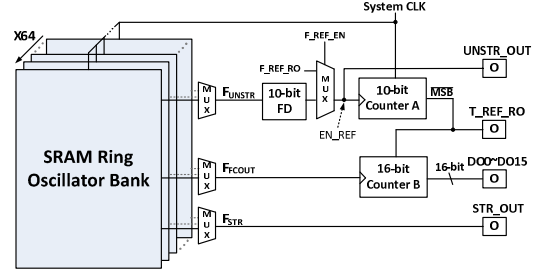


Fig. 9. The counter-based digital read-out measurement scheme.

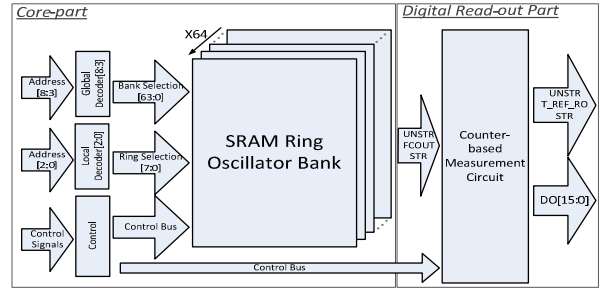


Fig. 10. Block diagram of the whole system.

cells for preserving the layout characteristics of SRAM cell array.

C. Counter-Based Measurement Circuit

Since the threshold voltage of MOSFET is an analog signal, it is difficult to extract large amount of data for SRAMs in SOCs. Hence, in this work, we use a full digital scheme to convert the threshold voltage drift to frequency difference to facilitate data extraction, processing, and statistical analysis. A basic set of measurement unit (Fig. 8) consists of two ring oscillators and a frequency comparator [10]. The output of the comparator, F_{COUT} , is the “Beat Frequency” (frequency difference between the stressed ring oscillator and the unstressed ring oscillator). The final stage of ESROs, the 101-stage enabling NAND gate, is placed in the frequency comparator block. A counter-based digital read-out scheme is used to convert the beat frequency to digital output. The detailed structure is shown in Fig. 9. With this scheme, we can extract the beat frequency quickly with high resolution.

As shown in Fig. 9, for NBTI in PMOS, the beat frequency F_{COUT} ranges roughly from 50 KHz to 760 KHz. Due to wide frequency range of F_{COUT} , the counter B (16-bit) should have the ability to cover the lowest and the highest frequency of F_{COUT} so that it won’t overflow in the counting period, which is decide by counter A (10-bit). The extracted digital data can be easily converted back to threshold voltage drift with a conversion table for statistical analysis.

One SRAM Ring Oscillator bank includes 8 sets of measurement unit. The core part of the measurement circuit (Fig. 9) comprises of 64 SRAM Ring Oscillator banks and some peripheral circuits, such as decoder, global MUX, and buffer. The system block diagram is shown in Fig. 10. The

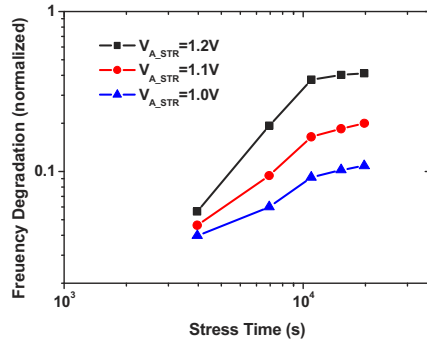


Fig. 11. Measured ESRO frequency degradation versus stress time for different NBTI stress voltage.

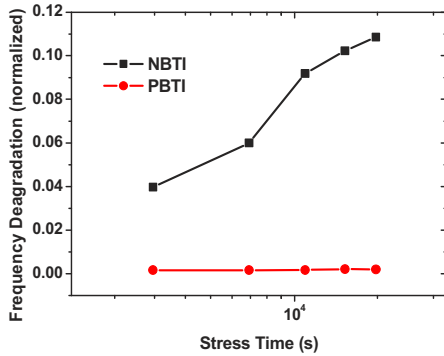


Fig. 12. Measured ESRO frequency degradation under NBTI-only and PBTI-only stress in $\text{SiO}_2/\text{poly-gate}$ technology.

inputs are 9-bit address and control signals like clock signal (CLK), and enable signal (EN) for ring oscillator. The lowest three bits of address, address [2:0] are for selecting one of the 8-set ESROs and beat frequency circuit in one bank. The [8:3] bits of address are used to select one of the 64 banks. The oscillating signals of F_{STR} , F_{UNSTR} and F_{FCOUT} are transmitted to the digital read-out circuit. STR and UNSTR are also transmitted to the chip output for observation. The area of the overall system, excluding the digital read-out circuit is $1650 \text{ um} \times 1050 \text{ um}$. The area of the digital read-out circuit is 903 um^2 , representing an area overhead of 0.52%

III. MEASUREMENT RESULTS

A test-chip is implemented in a 55nm $\text{SiO}_2/\text{poly-gate}$ standard performance bulk CMOS technology. The real-time frequency degradation of stressed ESRO can be observed by recording the counter output or directly observing the STR_OUT in Fig. 9. The external reference signal, F_{REF_RO} makes the digital read-out circuit more adaptive to wide range of beat frequency.

Fig. 11 shows the measured ESRO frequency degradation versus stress time for NBTI stress voltage of 1.2V, 1.1V and 1.0V. As expected, higher stress voltage, V_{A_STR} , results in larger frequency degradation. We find that the frequency degradation starts to saturate after 10^4 seconds stress time. Based on the frequency degradation vs. threshold voltage drift characteristics in Fig. 7, the threshold voltage drift of pull-up PMOS is more than 50mV after 10^4 seconds of 1.0V stress. Fig. 12 compares the measured results of NBTI stress and PBTI stress. Since $\text{SiO}_2/\text{poly-gate}$ technology is employed, the ESRO frequency is degraded after NBTI-only stress, while

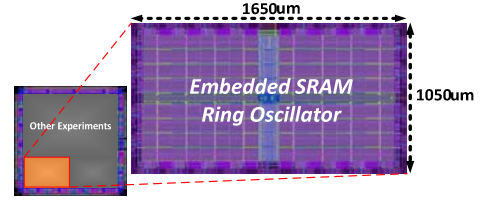


Fig. 13. Die photo (left) and layout view (right) of the test chip.

there is negligible change in ESRO frequency after PBTI-only stress. Fig. 13 shows the die photo and layout view for this test chip.

IV. CONCLUSION

In this work, we present an Embedded SRAM Ring Oscillator (ESRO) structure for measuring the degradation of 6T SRAM cell transistors induced by NBTI/PBTI. The ESRO preserves the original layout characteristics of 6T SRAM cell array with stress capability. We also describe the digital read-out scheme, and the measured BTI frequency degradation in 55nm standard performance CMOS technology.

ACKNOWLEDGMENT

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An All-Digital Read Stability and Write Margin Characterization Scheme for CMOS 6T SRAM Array

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Abstract—We present an all-digital Read Stability and Write Margin (WM) characterization scheme for CMOS 6T SRAM array. The scheme measures the cell Read Disturb voltage (V_{read}) and cell Inverter Trip voltage (V_{trip}) in SRAM cell array environment. Measured voltages are converted to frequency with Voltage Controlled Oscillator (VCO) and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. Resistor based voltage divider with 64 voltage levels and 10mV per step is employed to allow sweeping of BL voltage from 640mV to GND for WM characterization. A 512Kb test macro is implemented in UMC 55nm 1P10M Standard Performance (SP) CMOS technology. Monte Carlo simulations validate the accuracy of V_{read} and V_{trip} measurement scheme, and post-layout simulations show the resolution of the digital read-out scheme is 0.167mV/bit.

I. INTRODUCTION

The cell stability, Static Noise Margin (SNM) [1], and V_{MIN} of CMOS 6T SRAM are limited by leakage, variation, and supply voltage in the physical domain [2-7], and conflicting Read/Write requirements and cell disturb in the design domain. With technology scaling, the variations in cell Read-Disturb voltage (V_{read}) (Fig. 1) and cell Inverter Trip voltage (V_{trip}) increase, causing overlap and Read failure [8]. Various measurement techniques have been developed to characterize SRAM bit cell transistors, Read Stability and Write Margin (WM) [9]. While individual cell/device based characterization structures [10] can offer detail characteristics of the individual subjects, it is preferable and essential to characterize the Read Stability and WM in product array like environment so as to capture all the lithography and process related effects [11-14]. It is also important that the layout surrounding measured devices is as close as possible to the layout of the original SRAM array to incorporate the effects of dense layout and the applied ground rule waivers not present in isolated single transistor or cell.

In this work, we present an all-digital Read Stability and Write Margin (WM) characterization scheme for CMOS 6T SRAM array. The scheme measures the cell Read Disturb voltage (V_{read}) and cell Inverter Trip voltage (V_{trip}) in SRAM cell array environment. Measured voltages are converted to frequency with Voltage Controlled Oscillator (VCO) and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. Resistor based voltage divider with 64 voltage levels is employed to allow sweeping of BL voltage for WM characterization. Section II describes the modified cell structure, measurement scheme and Monte Carlo simulation results to validate the measurement scheme. Section III presents the test macro architecture and digital read-out

scheme. Section IV discusses the 512Kb test macro implementation in UMC 55nm CMOS technology. The conclusions of the paper are given in Section V.

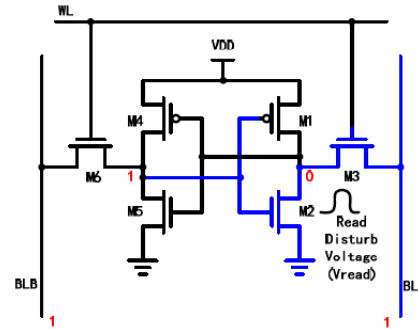


Fig. 1. Standard 6T SRAM cell in Read mode.

II. MEASUREMENT SCHEMES FOR V_{READ} , V_{TRIP} AND WM

A. Modified Cells for V_{read} and V_{trip}

Fig. 2 and Fig. 3 depict the schematic, modification of the cell layout and the equivalent circuit for V_{read} and V_{trip} measurement, respectively. For 6T SRAM, thin cell layout with horizontal uni-directional poly, and pattern density/symmetry are crucial for manufacturability and yield, especially for poly, diffusion and contact layers. To blank out unused cell devices and alter connections while preserving the layout and surroundings of critical layers, we keep the diffusion, poly and contact layers intact, and only modify Via and metal layers as shown in Fig. 2(b) and 3(b).

To measure V_{read} , the left cell inverter is blanked out with its supply and GND nodes left floating. The input of the right cell inverter (gate of M1/M2) is connected to V_{DD} to force the right cell storage node Q to “Low”, corresponding to the condition for Read operation. The column structure for V_{read} measurement is shown in Fig. 4(a). In V_{read} measurement mode, “ $V_{\text{read_enb}}$ ” goes “Low”, and the Read conditioning PMOS precharges and holds BL at V_{DD} . The voltage at node Q, resulting from the voltage divider effect from right access transistor M3 and right pull-down NMOS M2, will be V_{read} , and is passed through the left access transistor M6 to BLB for measurement.

For V_{trip} measurement, the left cell inverter is blanked out with its supply and GND nodes left floating. In V_{trip} measurement mode, “ $V_{\text{trip_enb}}$ ” (Fig. 4(b)) goes “Low”, The Trip conditioning PMOS equalizes (i.e. shorts) the voltages of BL and BLB, which in term forces the input and output of the right cell inverter (M1/M2 in Fig. 3) to equal potential at V_{trip} .

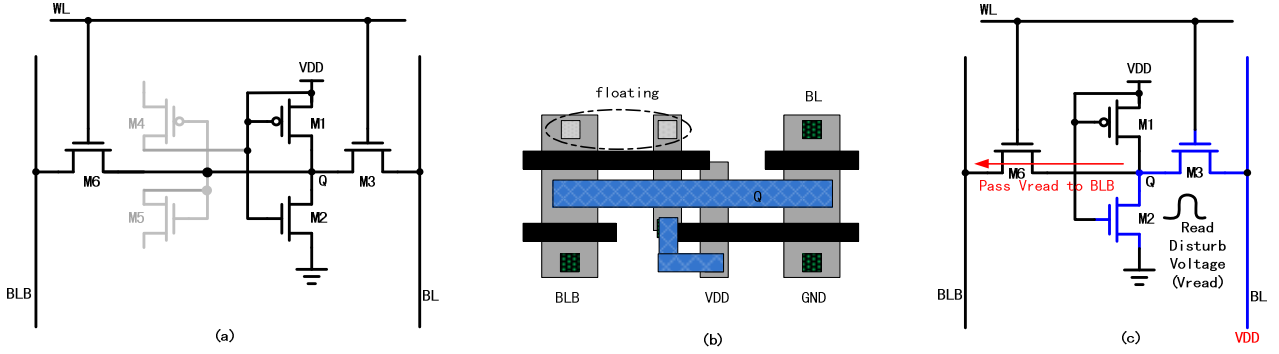


Fig. 2. (a) V_{read} cell schematic, (b) V_{read} cell layout and (c) V_{read} cell equivalent circuit.

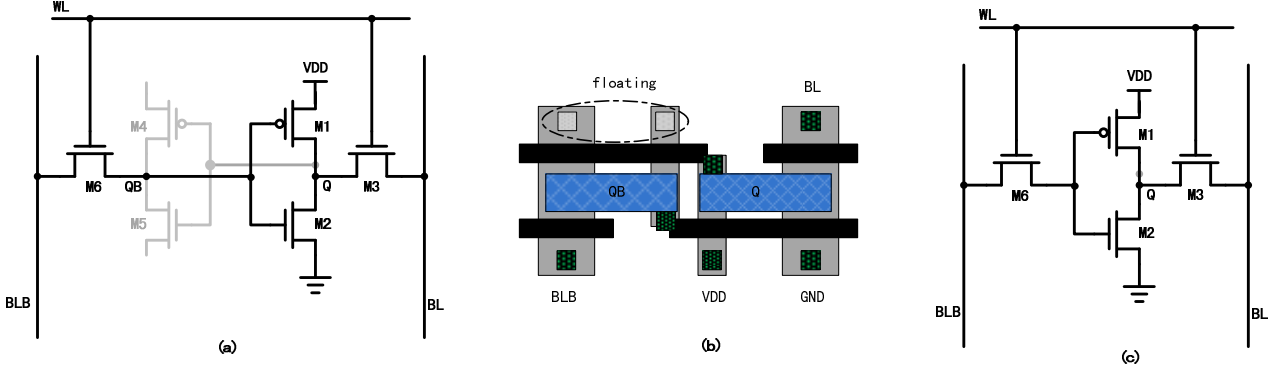


Fig. 3. (a) V_{trip} cell schematic, (b) V_{trip} cell layout and (c) V_{trip} cell equivalent circuit.

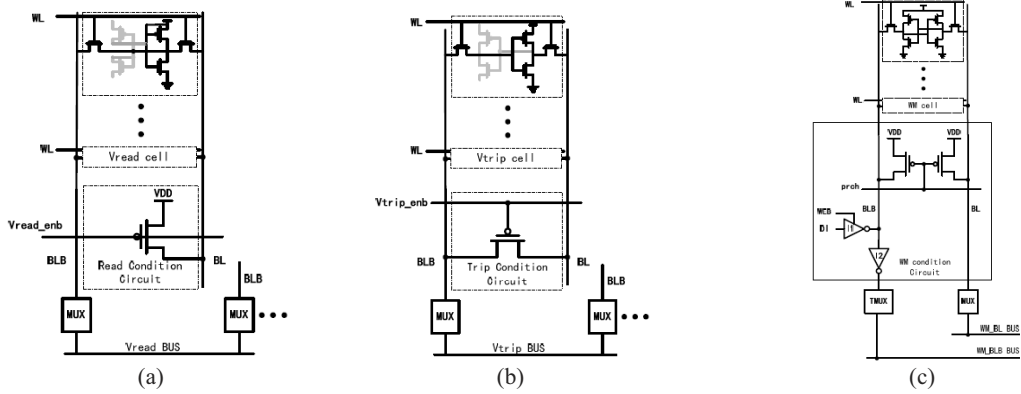


Fig. 4. Column structure for (a) V_{read} , (b) V_{trip} and (c) WM measurement.

Fig. 5 compares the Monte Carlo simulation results (290000 samples) of V_{read} and V_{trip} distributions of the proposed scheme with that of a single isolated cell inverter. The distribution of the proposed scheme can be seen to track that from single isolated cell inverter very well.

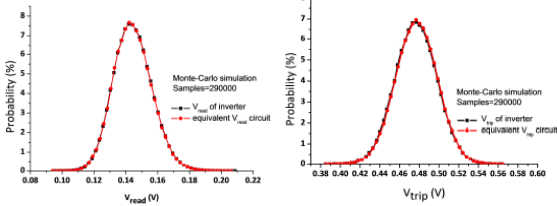


Fig. 5. Comparison of Monte Carlo simulation results for (a) V_{read} and (b) V_{trip} of proposed scheme with that of isolated cell inverter.

B. Write Margin (WM) measurement

Resistor based voltage divider with 64 voltage levels and 10mV per step is employed to allow sweeping of BL voltage from 640mV to GND for WM characterization. In WM measurement mode, background data of “1” ($Q = 1$) are written into the cell array. Then, “WEB (Write Enable BAR)” (Fig. 4(c)) goes “Low”, enabling gated inverter I1 to clamp BLB at V_{DD} . The output from the resistor based voltage divider is fed into BL through an unity gain buffer to “Write” the selected cell to “0”. “WEB” then goes “High” to disable gated inverter I1, and the data in the selected cell is sensed (i.e. Read) by sensing inverter I2 from BLB to decide whether the Write operation has been successfully performed.

III. TEST CHIP ARCHITECTURE AND DIGITAL READ-OUT SCHEME

Fig. 6 shows the measurement array architecture. To reduce pin count for the control signals and input address, shift registers are employed for both row and column decoders. The columns for V_{read} , V_{trip} , and WM measurement are interleaved with independent set of column shift registers. For WM measurement, it is necessary to stay at the same selected WL through Write (WM Measurement)-Read (Verify whether Write is successful)-Write (Write original data back into selected cells) sequence while sweeping through the BL voltage step. Two types of shift registers are employed: the column shift register (Fig. 7(a)) for normal sequential shift and the row shift register (Fig. 7(b)) with the added capability of holding the previous data (for staying at the same WL for WM measurement). To prevent the voltage level degradation through the column mux, full transmission gate with high gate control voltage of 1.2V is use. The rest of the design including supply for cell array operates at 1.0V.

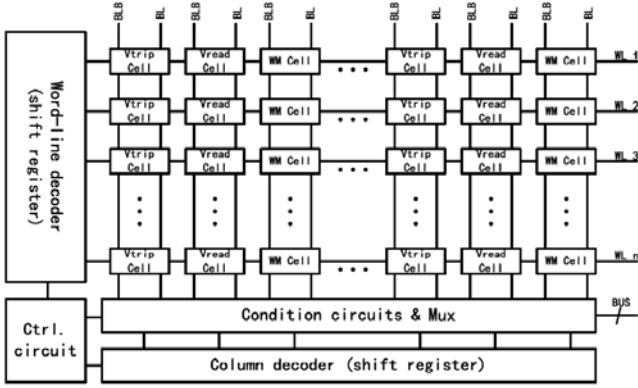


Fig. 6. Measurement Array Architecture.

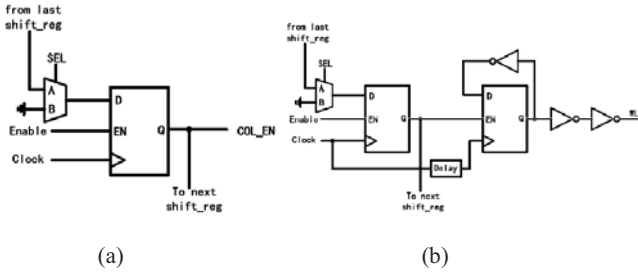


Fig. 7. (a) Column shift register and (b) row shift register.

The bit-line length is 128 cells. Each bank comprises 128 WL and 85 sets of interleaved V_{read} , V_{trip} and WM columns (a total of 3×85 columns). So there are about $128 \times 85 \times 3 \sim 32\text{K}$ cells in a bank. With 16 banks, the total cell number is $16 \times 32\text{K} \sim 512\text{Kb}$. For each V_{read} , V_{trip} or WM measurement, we can obtain $128 \times 85 \times 16 = 174.08\text{K}$ samples.

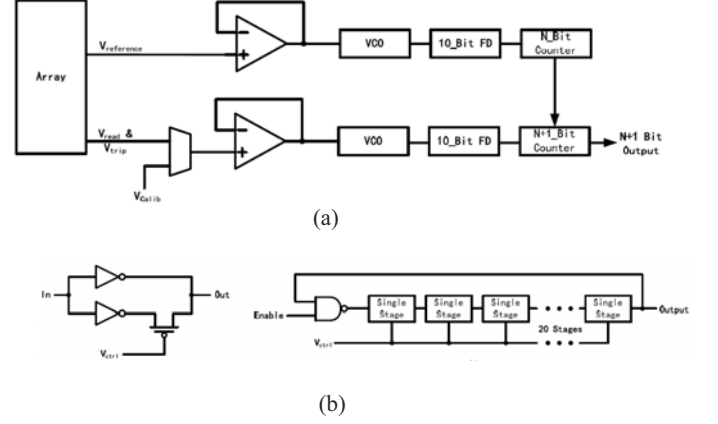
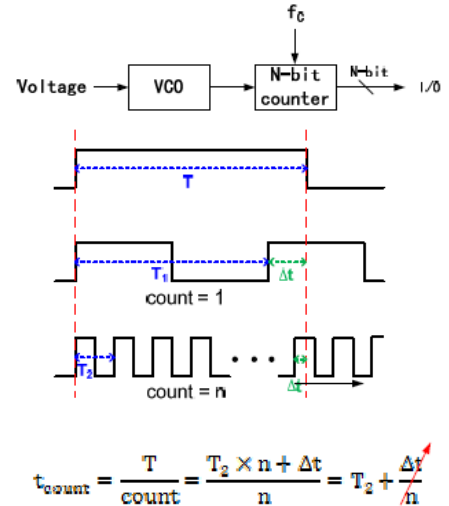


Fig. 8. (a) VCO and counter based digital read-out scheme and (b) single stage (left) of 21 stage VCO (right) [15].

To facilitate extraction, processing, and statistical analysis of large amount of data, a VCO (Voltage Controlled Oscillator) and counter based digital read-out scheme (Fig. 8 and 9) similar to that in [15] is employed. The measured analog voltage is fed into an unity-gain buffer, converted into frequency by VCO, divided through a 10-bit Frequency Divider (FD) and read-out by the counter. Reference and calibration paths are provided. Since the voltage levels of measured V_{read} and V_{trip} are low ($< 1/2 V_{\text{DD}}$), P-type VCO with PMOS delay control device (Fig. 8(b)) is employed so the measured analog voltage (the control voltage at the gate of PMOS delay control device) is at where the VCO sensitivity is maximum. This provides a sensitivity of about 480MHz/V (Fig. 10) for the VCO. The resolution of the counter depends on number of bits and the period of counting. The 13-bit counter in the Reference path is used to set the counting period of the 14-bit counter in the measurement path which does the actual counting. This provides a resolution of about 0.167mV/bit .



When n is large, $\Delta t/n$ can be ignored.

Fig. 9. Counting period and VCO resolution.

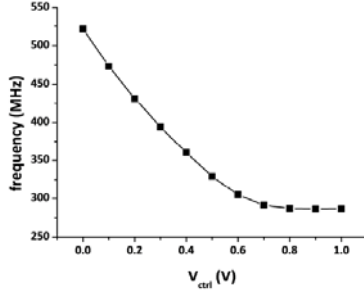


Fig. 10. Sensitivity of P-type VCO in Fig. 8(b).

IV. TEST MACRO IMPLEMENTATION

The 512Kb test macro is implemented in UMC 55nm 1P10M Standard Performance (SP) CMOS technology. This array based measurement macro is located at the upper right corner of the test chip (Fig. 11(a)). The layout view of the test macro is shown in Fig. 11(b)). The test array has two power domains: 1.2V for the full transmission gate column mux, and 1.0V for the cell array and other peripheral circuits. The total number of OP-Amp is 7 (2 for V_{read} measurement, 2 for V_{trip} measurement, 1 for resistor based voltage divider output for WM measurement, and 2 for calibration). All OP-Amps are located at the middle strip of the macro with a 3.3V supply. Four VCO's and resistor voltage divider are located at the right side of the macro with their own supply. The overall macro area is $2644 \mu\text{m} \times 1290 \mu\text{m}$ (excluding FD and counter) with 27 pins. The characteristics of the test macro are summarized in Table-I.

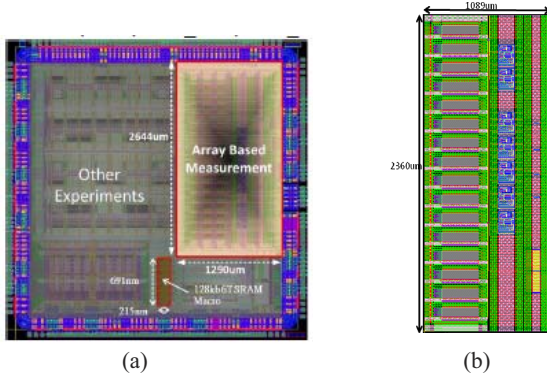


Fig. 11. (a) Array based measurement macro (upper right) in test chip and (b) layout view of array based measurement macro.

V. CONCLUSIONS

We presented an all-digital Read Stability and Write Margin (WM) characterization scheme for CMOS 6T SRAM array. The scheme measured the cell Read Disturb voltage (V_{read}) and cell Inverter Trip voltage (V_{trip}) in SRAM cell array environment. Measured voltages were converted to frequency with Voltage Controlled Oscillator (VCO) and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. A 512Kb test macro was implemented in UMC 55nm CMOS technology. Post-layout simulations showed the resolution of the digital read-out scheme is 0.167mV/bit.

Table-I : 512Kb Test Macro Characteristics

Capacity	Total 512 K bits
Process	55nm 1P10M SPRVT + HVT_6TSRAM
Area	
32 K-bit bank	445.9 $\mu\text{m} \times 150.7 \mu\text{m}$
OP	143.2 $\mu\text{m} \times 170.9 \mu\text{m}$
VCO	50.4 $\mu\text{m} \times 4.83 \mu\text{m}$
Overall	1290 $\mu\text{m} \times 2644 \mu\text{m}$ (excluding FD and counter)
Gain of VCO	482.2 MHz/V (@ $V_c=0\text{V}$)
	243.3 MHz/V (@ $V_c=0.6\text{V}$)
Resolution of Counter based measurement circuit	0.167 mV

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An All-Digital Bit Transistor Characterization Scheme for CMOS 6T SRAM Array

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Abstract—We present an all-digital bit transistor characterization scheme for CMOS 6T SRAM array. The scheme employs an on-chip operational amplifier feedback loop to measure the individual threshold voltage (V_{TH}) of 6T SRAM bit cell transistors (holding PMOS, pull-down NMOS, and access NMOS) in SRAM cell array environment. The measured voltage is converted to frequency with dual VCO and counter based digital read-out to facilitate data extraction, processing, and statistical analysis. A 512Kb test chip is implemented in 55nm 1P10M Standard Performance (SP) CMOS technology. Monte Carlo simulations indicate that the accuracy of the V_{TH} measurement scheme is about 2-7mV at TT corner across temperature range from 85°C to -45°C, and post-layout simulations show the resolution of the digital read-out scheme is < 0.2mV per bit. Measured V_{TH} distributions agree well with Monte Carlo simulation results.

I. INTRODUCTION

With technology scaling down to deep sub-100 nm regime, leakage, variation and long-term degradation have surfaced to constrain the stability, scalability and attainable performance of CMOS SRAM [1]. The rapid increase in local random V_{TH} variation, against the backdrop of lower supply voltage and increasing memory capacity in state-of-the-art processors and SoC, has become the major challenge in the design of 6T SRAMs. Various measurement techniques have been developed to characterize the V_{TH} fluctuation of logic devices [2-5] and SRAM bit cell transistors [6-8]. While isolated device/cell based characterization structures can offer detail characteristics of the individual subject, it is preferable and essential to characterize the V_{TH} variation in product array like environment to capture the lithography and process related effects. It is important to maintain the dense layout and surroundings of the measured devices as close as possible to the original SRAM array to incorporate the layout dependent effects and applied ground rule waivers not present in insulated single transistor. Various array based techniques for characterizing bit cell transistors and/or cell stability/degradation have been developed [7-12]. These array based techniques typically modify the SRAM cell layout to gain access to (or “expose”) the individual cell transistors for I_D and V_{TH} measurement in standard array topology without changing the cell layout considerably [8], or modify the SRAM column architecture to allow external access to each and every bit-line for gathering information on I_D and V_{TH} [7], Read Static Noise Margin (RSNM) and Write Margin (WM) by measuring bit-line current under various voltage sweeps [9, 10]. It is also highly desirable to have digital read-out scheme

to facilitate fast collection, extraction, processing, and statistical analysis of large amount of data [5, 12].

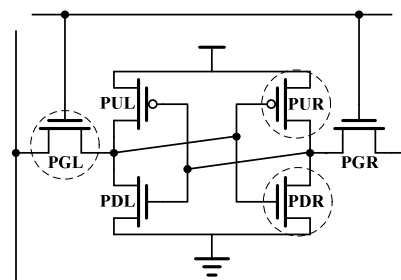


Fig. 1. Schematic of 6T SRAM cell.

In this work, we present an all-digital bit transistor characterization scheme for CMOS 6T SRAM array. The scheme employs an on-chip operational amplifier feedback loop to measure the individual threshold voltage of 6T SRAM bit cell transistors (holding PMOS, pull-down NMOS, and access NMOS) (Fig. 1) in SRAM cell array environment. The measured voltage is converted to frequency with dual-VCO and counter-based digital read-out to facilitate data extraction, processing, and statistical analysis. Section II describes the modified cell structure and measurement scheme. Section III presents the Monte Carlo simulation results and cell layout modification. Section IV discusses the test chip organization and peripheral circuit design. The digital read-out scheme is described in Section V. Section VI presents the 512Kb test chip implementation and measurement results in 55nm CMOS. The conclusions of the paper are given in Section VII.

II. MEASUREMENT SCHEME AND MODIFIED CELL STRUCTURE

Fig. 2 depicts the basic Operational Amplifier (OP-Amp) based V_{TH} measurement scheme in [2, 3], where the Device Under Test (DUT) is an NMOS (Fig. 2(a)) and a PMOS (Fig. 2(b)). In this scheme, the source voltage of DUT (V_{source}) follows V_{set} , and together with R_{load} , determines the current through DUT. The V_{set} and R_{load} are chosen such that the current density through DUT is where the V_{TH} is defined (and to be measured). As such, the gate voltage of DUT, V_{gate} , is one $|V_{TH}|$ above (below) V_{source} for NMOS (PMOS), and measurement of V_{gate} provides direct information of V_{TH} ($V_{gate} = V_{set} \pm |V_{TH}|$). This scheme has been used to characterize V_{TH} variations of an addressable array of 65nm PD/SOI logic transistors [2, 3].

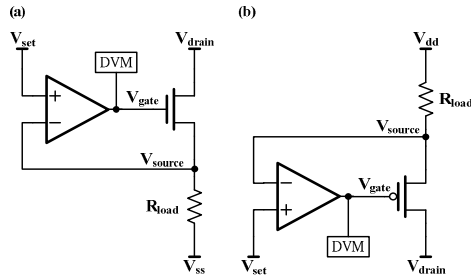


Fig. 2. Basic OP-Amp based V_{TH} measurement scheme, where the Device Under Test (DUT) is (a) NMOS and (b) PMOS [2, 3].

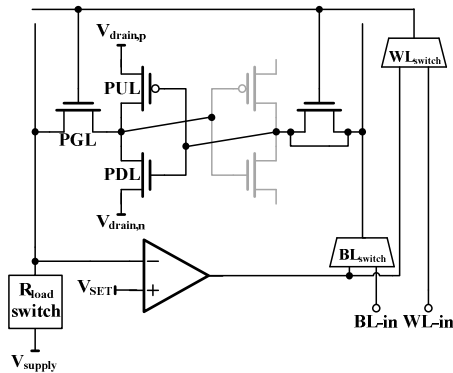


Fig. 3. Proposed OP-Amp based scheme for V_{TH} measurement of holding PMOS, pull-down NMOS and access NMOS in 6T SRAM cell array.

Fig. 3 shows the proposed OP-Amp based scheme for V_{TH} measurement of cell holding PMOS, pull-down NMOS and access NMOS in 6T SRAM cell array. The DUTs are PUL, PDL and PGL of the left-half cell. The right-half cell inverter is blanked out, and the source and drain of right access NMOS (PGR) are shorted to allow access to DUTs from the right BL without suffering the V_{TH} drop and variation through PGR. A R_{load} switch bank is provided so a proper value of R_{load} can be selected for V_{TH} measurement of each DUT (i.e. PUL, PDL and PGL). Table-I shows the measurement modes and respective control signals.

To measure V_{TH} of PUL (PUL mode), the right BL connects the PUL/PDL gate node and the OP-Amp output node, and the left BL connects R_{load} and the OP-Amp negative input. V_{supply} is tied to V_{DD} . The OPA positive input node holds at V_{SET} . The WL is asserted at a high voltage to mitigate the V_{TH} loss and variation through PGL. When WL goes high and the OP-Amp switches on, negative feedback loop keeps left BL (and the left cell storage node) at V_{SET} , and $(V_{supply} - V_{SET}) / R_{load}$ sets the bias current which defines V_{TH} . $V_{drain,n}$ is kept at V_{SET} so V_{DS} of PDL would be 0 to eliminate its leakage current. $V_{drain,p}$ connects to GND, so PUL operates in the inverse mode (S/D exchanged). The voltage of right BL (corresponding to V_{gate} in Fig. 2(b), at $V_{SET} - |V_{TH}|$) is the output of measurement. The measurement of V_{TH} of PDL (PDL mode) operates in complementary manner.

Table-I : Measurement Mode and Control Signal

Signal	PUL Mode	PDL Mode	PGL Mode
$V_{\text{drain,p}}$	GND	V_{SET}	V_{DD}
$V_{\text{drain,n}}$	V_{SET}	V_{DD}	V_{DD}
$\text{BL}_{\text{switch}}$	OPA-out	OPA-out	BL-in
$\text{WL}_{\text{switch}}$	WL-in	WL-in	OPA-out
V_{supply}	V_{DD}	GND	GND

Note: $V_{DD} = 1.0V$, $GND = 0V$, V_{SET} varies for each mode.

To measure V_{TH} of PGL (PGL mode), the OP-Amp output is connected to the gate of PGL through WL_{switch} (Mux). Both $V_{drain,p}$ and $V_{drain,n}$ are kept at V_{DD} , and logic “0” is passed from BL-in through BL_{switch} to right BL, and then to the input of left cell inverter to set the left cell storage node at V_{DD} . In this case, both PUL and PDL hold the left cell storage node at V_{DD} , and there is no leakage current through them as their $V_{DS} = 0V$. V_{supply} ties to GND, and the bias current is set at $(V_{SET} - GND) / R_{load}$.

III. MONTE CARLO SIMULATION RESULTS AND CELL LAYOUT MODIFICATION

Fig. 4 compares the Monte Carlo simulation results (290000 samples) of V_{TH} distributions of the proposed scheme and that of a single isolated cell device for PUL, PDL and PGL. The distribution of the proposed scheme can be seen to track that from single isolated cell device well. The discrepancy ranges from 2-7mV at TT corner across temperature range from 85°C to -45°C.

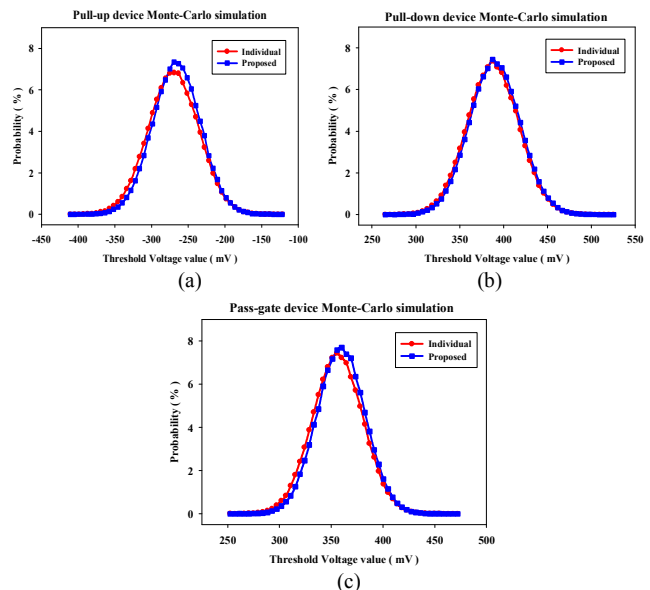


Fig. 4. Comparison of Monte Carlo simulation results of V_{TH} distribution of the proposed scheme and that of a single isolated cell device for (a) PUL, (b) PDL and (c) PGL at TT, 25°C.

For 6T SRAM, thin cell layout with horizontal unidirectional poly, and pattern density/symmetry are crucial for manufacturability, especially for poly, diffusion and contact layers. To blank out unused cell devices and alter connections while preserving the layout and surroundings of critical layers,

we keep the diffusion, poly and contact layers intact, and only modify Via and metal layers as shown in Fig. 5.

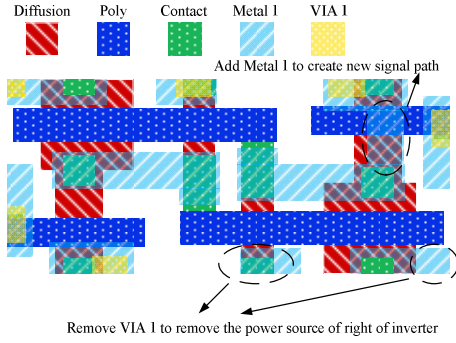


Fig. 5. Modification of 6T cell layout to form the proposed structure.

IV. CHIP ORGANIZATION AND PERIPHERAL DESIGN

The 512Kb test chip comprises eight 64Kb banks. The organization of a 64Kb bank is shown in Fig. 6, together with the Word-Line (Row) selection circuit and R_{load} switching circuit. The R_{load} switching circuit consists of 3 resistors, with resistance values optimized for PUL/PDL/PGL mode, respectively. The mode switch employs stacked switching transistors to ensure that the leakage through the unselected paths (modes) is suppressed well below the selected one (whose current is set at where V_{TH} is defined).

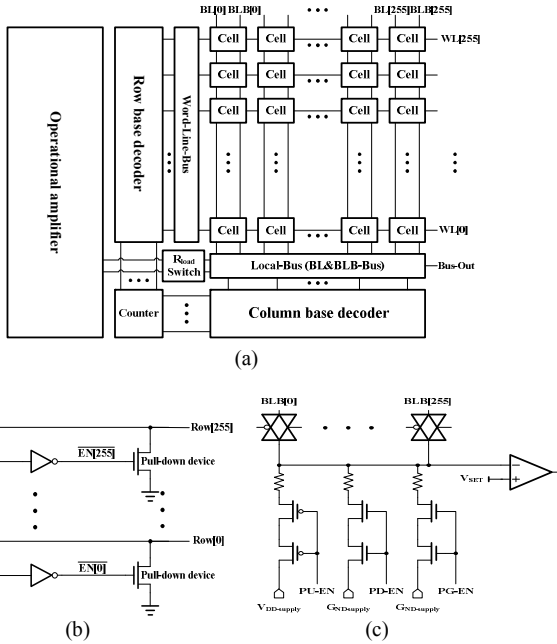


Fig. 6. (a) Organization of a 64Kb bank, (b) Word-Line (Row) selection circuit and (c) R_{load} switching circuit.

V. DIGITAL READ-OUT SCHEME

To facilitate extraction, processing, and statistical analysis of large amount of data, a VCO (Voltage Controlled Oscillator) and counter based digital read-out scheme (Fig. 7) similar to that in [5] is employed. The measured analog voltage is fed into an unity-gain buffer, converted into

frequency by VCO, and read-out by the counter. Reference and calibration paths are provided. Since both NMOS (PDL/PGL) and PMOS (PUL) are measured, the output from the measurement scheme in Fig. 3 has distinctly different voltage level for each mode and varies significantly across process and temperature corners. As such, two types of VCO are designed to provide maximum sensitivity for each mode and corner. The VCO has 30 stages. For the N-type VCO (Fig. 8(a)), when the control voltage (V_{ctrl}) rises, the VCO frequency increases (Fig. 9(a)). The P-type VCO (Fig. 8(b) and 9(b)) operates in complementary manner. The dual VCO design allows us to place the measured analog voltages (which are buffered then fed to V_{ctrl}) at where the VCO sensitivity (slopes of curves in Fig. 9) is maximum. Post-simulations based on 55nm Standard Performance CMOS technology show that we can achieve about 265MHz/mV for N-type VCO and 350MHz/mV for P-type VCO.

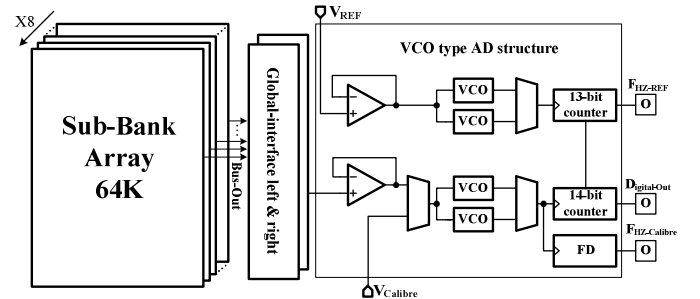


Fig. 7. Architecture of VCO and counter based digital read-out scheme.

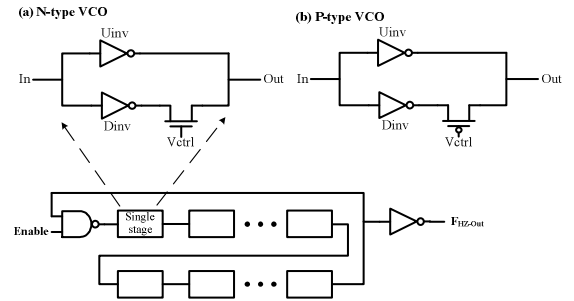


Fig. 8. Single stage of (a) N-type VCO and (b) P-type VCO.

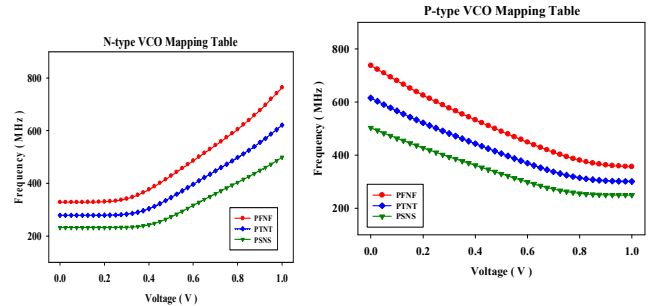


Fig. 9. Post-sim results of sensitivity for (a) N-type VCO and (b) P-type VCO.

The resolution of the counter depends on number of bits and the period of counting. The 13-bit counter in the Reference path is used to set the counting period of the 14-bit counter which does the actual counting. This provides a resolution of about 0.125mV (0.12mV) per bit when N-type (P-type) VCO

is used.

VI. 512Kb TEST CHIP IMPLEMENTATION

The 512Kb test chip is implemented in 55nm 1P10M Standard Performance (SP) CMOS technology. The layout view is shown in Fig. 10 and the characteristics of the test chip are summarized in Table-II. The overall chip area is $1800 \mu\text{m} \times 930 \mu\text{m}$ with 24 pins and 7 power domains (1.0V for cell supply, 1.2V for peripheral, 3.3V for OP-Amp, 3 supplies for V_{SET} , 1 for higher WL-in). Fig. 11 shows the measured V_{TH} distributions, which agree well with Monte Carlo simulation results.

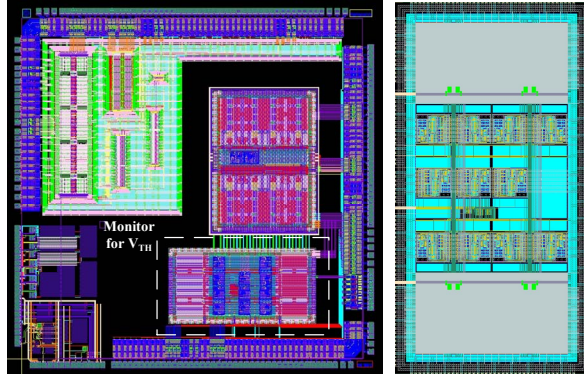


Fig. 10. Layout view of the die (Left) and the 512Kb test chip (Right).

Table-II : 512Kb Test Chip Characteristics

Capacity	Total 512Kbits
Process	55nm 1P10M SP RVT/HVT
Analog-to-Digital Circuit Scheme	
Measurement range	15us ~ 30us
Resolution	0.125mV for n-type / 0.12mV for p-type
Area	
64Kbit Bank	585.2 $\mu\text{m} \times$ 183.3 μm
OPA	143.2 $\mu\text{m} \times$ 170.9 μm
A/D Circuit Scheme	52.2 $\mu\text{m} \times$ 151.9 μm
Overall	1800 $\mu\text{m} \times$ 930 μm

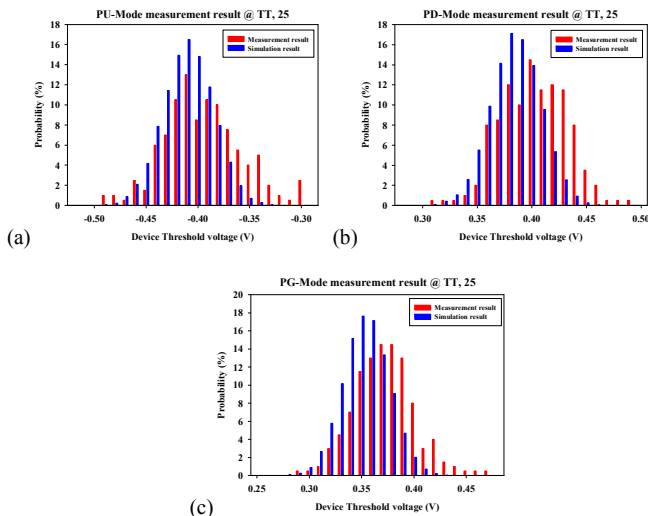


Fig. 11. Measured V_{TH} distributions of (a) PUL, (b) PDL and (c) PGL at TT, 25°C. Monte Carlo simulation results are also shown for comparison.

VII. CONCLUSION

We presented an all-digital bit transistor characterization scheme for CMOS 6T SRAM array. The scheme employed an on-chip operational amplifier feedback loop to measure the individual threshold voltage of 6T SRAM bit cell transistors in cell array environment. Dual VCO and counter based digital read-out scheme provided high sensitivity and resolution, and facilitate data extraction, processing, and statistical analysis. A 512Kb test chip was implemented in 55nm Standard Performance CMOS technology. Monte Carlo simulations indicated that the accuracy of the scheme is about 2-7mV at TT corner across temperature range from 85°C to -45°C, and post-layout simulations showed the resolution of the digital read-out scheme is $< 0.2\text{mV}$ per bit. Measured V_{TH} distributions agree well with Monte Carlo simulation results.

ACKNOWLEDGMENT

This work was supported by National Science Council, Taiwan, under Contract NSC 99-2221-E-009-183-MY2, Ministry of Economic Affairs in Taiwan under Contract 99-EC-17-A-01-S1-124, and Ministry of Education in Taiwan under ATU Program.

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