

A New Twin-Well CMOS Process Using Nitridized-Oxide-LOCOS (NOLOCOS) Isolation Technology

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Abstract—A new twin-well CMOS process using the nitridized pad-oxide film as a buffer layer for the enhanced local oxidation of silicon (LOCOS) has been developed in which the nitridized pad oxide is used to obtain a defect-free and near-zero bird's beak field isolation structure. The principal feature of the developed novel process is that high-temperature nitridation of thin pad oxide is simultaneously used to increase the junction depth of the As-implanted n-well. Both n- and p-channel MOSFET's fabricated by the developed twin-well CMOS process using the nitridized-oxide-LOCOS (NOLOCOS) isolation technology have been characterized and compared with those fabricated by the conventional LOCOS isolation technique. The major features of the developed NOLOCOS isolation technology in CMOS/VLSI fabrication have been clearly demonstrated.

I. INTRODUCTION

THE local oxidation of silicon (LOCOS) with a thin pad oxide as a buffer layer between the silicon-nitride mask and the silicon substrate has been widely used for device isolation between active MOSFET's [1]. However, this isolation technology always produces a large bird's beak length, which not only consumes a large amount of layout area but also results in serious narrow-width effects. Recently, several new isolation techniques using the nitridized pad oxide as the buffer layer have been proposed [2], [3]. It has been shown that using the thermally nitridized thin-oxide film, the silicon surface can be sealed without oxidation and used effectively to eliminate the bird's beak without producing the high-intrinsic nitride stress during high-temperature oxidation [4], [5].

In this paper, the nitridized-oxide-LOCOS (NOLOCOS) technology developed previously [1], [3] has been applied to CMOS fabrication. In order to fully utilize the high-temperature process during thermal nitridation of oxide, a new twin-well CMOS process has been developed to demonstrate the advantages of the NOLOCOS technology in CMOS/VLSI fabrication.

II. A TWIN-WELL CMOS PROCESS USING THE NOLOCOS TECHNOLOGY

The major fabrication steps of the developed twin-well CMOS process are shown in Fig. 1. The n-well was initially

formed by a high-energy (190 keV) arsenic ion implantation followed by a subsequent drive-in at 1200°C in an N₂ ambient for 3 h, as shown in steps ① and ②. After stripping the sacrificed oxide (500 Å), the thin pad oxide (150 Å) was grown and then nitridized in an ammonia ambient at 1200°C for 7 h which drove the n-well deeper.

A LPCVD-Si₃N₄ layer (700 Å) was then deposited. Using a photolithographic step ③, the nitride and oxynitride layers were patterned for LOCOS oxidation. Note that a zero alignment key was used and the misalignment tolerance was about 0.3 μm. The field oxide (7500 Å) was grown in a pyrogenic steam ambient with 6-percent HCl mixture and *in-situ* annealed to release the residual stress at the field oxide edge. Using a 2.5-μm-thick photoresist layer over the n-well region as an implantation mask, high-energy doubly charged boron ions (B⁺⁺) with an energy of 195 keV and a dose of $6 \times 10^{12}/\text{cm}^2$ were implanted into the p-substrate region for both shallow retrograde p-well formation [6] and p-field threshold-voltage adjustment, as shown in step ④. Note that a punchthrough implant for an n-channel MOSFET under the same photoresist layer and a blanket implant after the removal of the photoresist were performed to adjust the channel threshold voltage. It is clearly seen that a mask layer for channel implant is eliminated. After the proper annealing steps and a sequence of conventional n⁺-doped poly-gate CMOS back-end processes, twin-well CMOS transistors with process parameters listed in Table I were fabricated, as shown in step ⑤. It should be noted that twin-well CMOS transistors using conventional CMOS process were also fabricated for comparison. For the p-well, the channel surface concentrations of NOLOCOS and conventional LOCOS are $7 \times 10^{16}/\text{cm}^3$ and $6 \times 10^{16}/\text{cm}^3$, respectively. For the n-well, the channel surface concentrations of NOLOCOS and conventional LOCOS are $2.22 \times 10^{16}/\text{cm}^3$ and $1.8 \times 10^{16}/\text{cm}^3$, respectively. The process parameters for both technologies are listed in Table I.

III. DEVICE CHARACTERISTICS

The fabricated CMOS transistors using the NOLOCOS technology have been characterized and compared with those using the conventional LOCOS technology.

A. Effective Channel Width

W_{mask} and the effective dimension loss of channel width $\Delta W_{\text{eff}} \Delta W_{\text{eff}} = W_{\text{mask}} - 2 \Delta W_{\text{eff}}$, where ΔW_{eff} is mainly due

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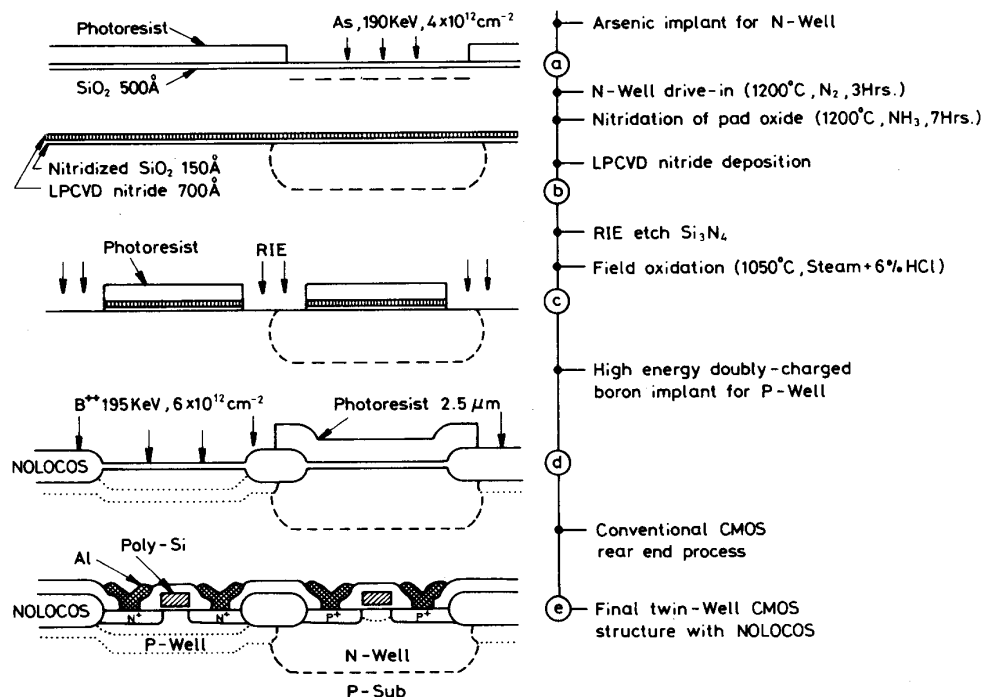


Fig. 1. Major fabrication steps of the proposed twin-well CMOS process using the NOLOCOS technology.

TABLE I
PROCESS PARAMETERS FOR BOTH CMOS/NOLOCOS AND CMOS/LOCOS

Process Data	Tox (Å)	Tfox (Å)	Xj (μm)			P-field Implant	Channel Implant	
			N-Well	n*	p*		I (Blank)	II (n-channel)
NOLOCOS	140	7500	3.5	0.25	0.3	B ⁺⁺ , 195 KeV 6 x 10 ¹² cm ⁻²	B ⁺ , 25 KeV 1.5 x 10 ¹² cm ⁻²	B ⁺ , 50 KeV 1 x 10 ¹² cm ⁻²
LOCOS	140	7500	4.5	0.25	0.3	B ⁺ , 25 KeV 3 x 10 ¹³ cm ⁻²	B ⁺ , 25 KeV 2 x 10 ¹² cm ⁻²	

to the photolithographic process, reactive ion-etching process, bird's beak length, and lateral diffusion of field implantation. Comparisons of the measured linear transconductances G_m between the NOLOCOS and the LOCOS for CMOS transistors with various channel widths are shown in Fig. 2. The effective channel-width improvements for both p- and n-MOSFET's using the NOLOCOS are extracted to be 1.0 and 1.2 μm , respectively. Note that the dimensional loss due to bird's beak length is less than 0.1 μm [2] and that due to lateral diffusion is only about 0.05 μm for both p-well and n-well regions. Therefore, the dimensional loss excluding the loss due to the photolithographic process (0.2 μm each side) is only 0.15 μm , which is consistent with that measured from the SEM cross-section view [2].

B. Threshold Voltage

The improvements of the narrow-width effects on the threshold voltages of CMOS transistors using the NOLOCOS are shown in Fig. 3. The threshold-voltage variations (ΔV_{th}) of both n- and p-MOSFET's using the NOLOCOS are within 40 and 120 mV, respectively, for W_{mask} down to 1.5 μm . On

the other hand, the ΔV_{th} of those devices using the LOCOS are widely spread to more than 200 mV for W_{mask} narrower than 3 μm . Under the back-gate bias of 3 V, the ΔV_{th} variations of both n- and p-MOSFET's using the NOLOCOS are within 40 and 160 mV, respectively, while those devices using the LOCOS are widely spread to more than 400 mV for W_{mask} narrower than 3 μm . The improvements on ΔV_{th} of n-MOSFET are due to the reduction of the lateral diffusion of p-field impurity using high-energy doubly charged B⁺⁺ implantation, and those of p-MOSFET are due to the reduction of the lateral diffusion of n-field impurity using arsenic implantation instead of phosphorus for n-well doping.

C. Isolation Property

The subthreshold I - V characteristics of the CMOS field transistors with $(W/L)_{\text{mask}} = 30 \mu\text{m}/2 \mu\text{m}$ are shown in Fig. 4, in which the threshold voltages of both n- and p-channel field MOS transistors are $V_{thfn} = 13.7 \text{ V}$ and $V_{thfp} = -18.3 \text{ V}$, respectively. It is shown that the leakage current is in subpicoamperes. Therefore, the field isolation of the NOLOCOS technology is excellent.

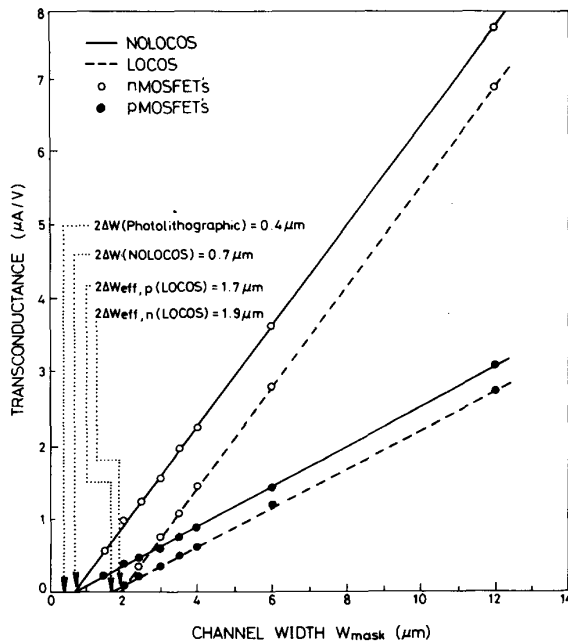


Fig. 2. Comparisons of the linear transconductances of CMOS transistors with various channel widths between NOLOCOS and conventional LOCOS isolation technologies.

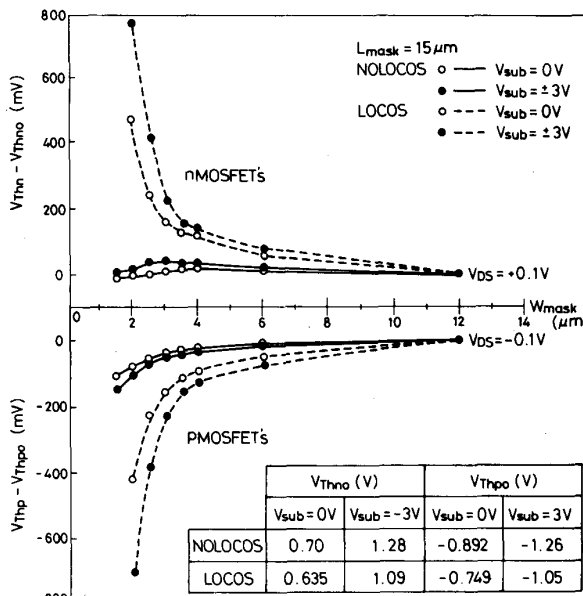


Fig. 3. Comparisons of the narrow-width effects on the threshold voltage of CMOS transistors between NOLOCOS and conventional LOCOS isolation technologies.

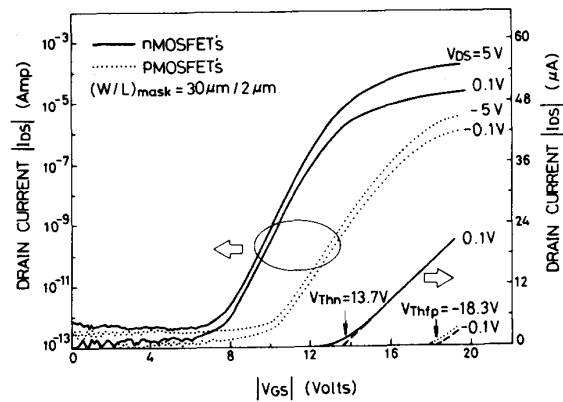


Fig. 4. Isolation property of CMOS field transistors fabricated using the NOLOCOS technology.

IV. CONCLUSION

A new twin-well CMOS process using the NOLOCOS technology has been developed. This novel CMOS process with arsenic ion implantation for the n-well and doubly charged B⁺⁺ ion implantation for the retrograde p-well is shown to fully utilize the high-temperature NOLOCOS isolation technology and eliminates one mask layer as compared to the conventional twin-well process. Through device characterization, it has been shown that the developed twin-well CMOS process using the NOLOCOS technology offers a fairly large recovery of the effective channel width, very good device isolation properties, and very small narrow-width effects. These features are beneficial for scaled CMOS/VLSI fabrication.

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