

A Quasi-Two-Dimensional Analytical Model for the Turn-On Characteristics of Polysilicon Thin-Film Transistors

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Abstract—A physical model considering the effects of grain boundaries on the turn-on behavior of polysilicon thin-film transistor's (poly-Si TFT's) is presented. Along the channel, the formation of the potential barrier near the grain boundary is proposed to account for the low transconductance and high turn-on voltage of TFT's. The barrier height is expressed in terms of channel doping, gate oxide thickness, grain size, and external gate as well as drain biases. Drain bias will result in an asymmetric potential barrier and introduce more carrier injection from the lowered barrier side. It is shown that this consideration is very important to characterize the saturation region under large drain-bias condition. Based upon the developed potential barrier model, the I - V characteristics are described by the interfacial-layer thermionic-diffusion model. Moreover, thin-film transistors on polycrystalline silicon with a coplanar structure were fabricated for testing. Comparisons between the developed model and the experimental data have been made and excellent agreement has been obtained.

NOMENCLATURE

Ψ	Two-dimensional potential distribution.
$\epsilon_{si} (\epsilon_{ox})$	Dielectric permittivity of Si (SiO ₂).
Ψ_{so}^i	The potential distribution at the point (0, 0) in the i th grain as shown in Fig. 1.
V_i	Quasi-Fermi level difference between the source and the i th grain in the channel.
N_A	Average doping concentration in the p-type substrate.
C_{ox}	Gate oxide capacitance per unit area.
V_{FB}	Flat-band voltage.
y_d	Depletion depth.
$x_{d\mp}^i$	Lateral width of the space-charge region on the left (−)/right (+) side of the i th grain boundary as shown in Fig. 1.
E_L^i	Lateral electric field emanating from the drain.
N_{st}	Trapping density at the grain boundary.
Q_{GB}	Areal density of the charges trapped at the grain boundary.
E_T	Trap energy level.
E_i	Intrinsic energy level.

E_F^i	Quasi-Fermi level in the i th grain.
$\Psi_{B\mp}^i$	Barrier height on the left (−)/right (+) side of the i th grain boundary as shown in Fig. 1.
ϕ_{sinv}	Surface band-bending at the onset of strong inversion.
y_{dinv}	Depletion depth at the onset of strong inversion [$= (2\epsilon_{si}\phi_{sinv}/qN_A)^{1/2}$].
V_{To}	Intrinsic threshold voltage of TFT's without the effect of charge coupling between the grain boundary and the gate voltage.
V_T	Threshold voltage of TFT's with finite grain size.
$n(0, 0)$	Electron density at the point (0, 0) in Fig. 1.
V_{dp}^i	Voltage drop across the lateral depletion region of the i th grain.
δV_i	Voltage drop across the i th grain
m_n^*	Effective conduction mass of electrons.
θ_n	Transmission coefficient of electrons across the grain boundary.
v_{Rn}	Thermal velocity of electrons across the grain boundary ($= [K_B T/2\pi m_n^*]^{1/2}$).
$\theta_n v_{Rn}$	Effective velocity of electrons across the grain boundary.
v_{nD}^i	Effective diffusion velocity of electrons in the space-charge region of the i th grain.
β	Inverse of the thermal voltage ($= q/K_B T$).
L_g	Average grain size.
N_g	Total number of grains distributed in the channel.
W_T^i	Total lateral width of the space-charge region in the i th grain.
μ_n	Electron mobility in the surface channel.
μ_0	Maximum electron mobility in the surface channel.
θ	Empirical constant for surface-roughness scattering.
v_{sl}	Scattering-limited velocity.

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I. INTRODUCTION

RECENTLY, polycrystalline silicon thin-film transistors (poly-Si TFT's) have been extensively studied because of their important applications in flat-panel dis-

play and three-dimensional integration [1], [2]. Due to the formation of the grain boundaries along the channel, the characteristics of poly-Si TFT's show much smaller transconductance and larger threshold voltage than those of single-Si MOSFET's [3]–[7]. Fossum and Ortiz-Conde [5] had proposed a model in which the barrier height in the channel under the condition of large gate bias was related to the difference in carrier concentration between the inversion region and the depletion region near the grain boundary. Their model, however, largely overestimates the barrier height as the gate bias is around the threshold voltage. Due to this deficiency, Serikawa *et al.* [6] had modified Fossum's model by using an empirical formula to fix the potential barrier height to 0.55 V at the threshold voltage in order to characterize the current-voltage relation biased below the saturation region. However, the threshold voltage dependence on trapping density and grain size was not well discussed and was simply treated as a fitting parameter. Moreover, the drain current predicted by their model will level off before the saturation point due to the fact that the grain barrier dependence on the drain voltage is overlooked. Anwar and Khondker [7] had taken the effects of the grain size on the potential barrier height into consideration and discussed the characteristics of the threshold voltage and the conductance of TFT's with finite grain size. Their model, which is based upon a simplified numerical analysis, only takes into account the charge coupling between the gate and the grain boundaries. However, the effects of drain bias on the barrier height are still overlooked. It will be shown later that the drain bias will result in the asymmetric grain barrier and introduce more carrier injection from the lowered barrier side. This important effect is called the drain-induced grain barrier lowering (DIGBL) effect, which is shown to be a key factor in characterizing the exponential dependence of the drain current on the drain voltage for poly-Si TFT's operated at large drain voltage.

In this paper, we present a quasi-two-dimensional analytical model for the threshold voltage and the potential barrier height in the channel of poly-Si TFT's by considering crystalline structures from small to large grain sizes. The asymmetric barrier height modulated by the drain bias also has been considered. Based upon the developed potential barrier model, the current-voltage characteristics of poly-Si TFT's biased at the turn-on region have been described by the interfacial-layer thermionic-diffusion model. Finally, theoretical simulations have been compared with experimental data.

II. BARRIER HEIGHT AND THRESHOLD VOLTAGE

The formation of a potential barrier in the polycrystalline Si substrate channel is due to the fact that carriers are trapped at the localized grain-boundary states, and in turn, these trapped charges deplete free carriers near the grain boundaries. This charge-trapping process is almost the same as that of the bulk, except that the trapped charges are influenced by the gate bias. For a p-type poly-Si substrate, holes are trapped at the grain bound-

aries. When a positive voltage with respect to the substrate is applied to the gate, the energy band is bent down toward the Si-SiO₂ interface. The traps distributed in the regions where the trap level moves closer to the Fermi level are gradually filled by induced electrons. Thus, some of the total electric-flux lines emanating from the gate are terminated by the trapped charges in the grain boundaries and some by the bulk ionized charges. The potential barrier height, therefore, must be characterized by a two-dimensional solution of Poisson's equation.

A cross-sectional view of a poly-Si TFT with uniform grain doping is shown in Fig. 1; only the *i*th grain boundary and its nearby grains are shown for simplicity. In the shaded region, free carriers are depleted by the trapped charges in the grain boundaries; the two-dimensional Poisson's equation can be written as

$$\frac{\partial^2 \Psi}{\partial x^2} + \frac{\partial^2 \Psi}{\partial y^2} = \frac{qN_A}{\epsilon_{si}} \quad (1)$$

in which the boundaries of the shaded region are defined as follows: boundary 1 is located at the depletion edge where the boundary potential exhibits a maximum with zero lateral electric field for either partially or completely depleted grain. Although boundary 1 may not be straight line at higher drain bias, it is still a good approximation to simplify the analysis; boundary 2 is located at the Si-SiO₂ interface; boundary 3 is located at the grain boundary where carriers are trapped at the localized states; boundary 4 is located at the depletion region edge (y_d), below which the depletion charges belong to the grain boundary in the bulk. Since the electric field direction is almost lateral at the depletion edge y_d , it is reasonable to assume the normal electrical field at $y = y_d$ is zero. Moreover, it is assumed that y_d is independent of x for simplicity.

Applying Gauss's theorem to a volume enclosed by the planes located at these boundaries [8], we get

$$-\frac{C_{ox}}{\epsilon_{si}} \int_0^x [V_{GS} - V_{FB} - \Psi(x', 0)] dx' - \int_0^{y_d} \frac{\partial}{\partial x} \Psi(x, y') dy' = -\frac{qN_A y_d x}{\epsilon_{si}}. \quad (2)$$

It should be noted that if the variation of y_d with respect to x is not significant within a single grain, the resulting error for the grain barrier in the surface layer can be smeared out due to the integration process in (2). Under the same assumptions, the potential function can be expressed as $\Psi(x, y) \equiv \Psi(0, y) + \phi(x) (1 - (y/y_d))^2$. Substituting the above relation into (2) and differentiating both sides with respect to x , we have

$$\frac{\partial^2}{\partial x^2} \phi(x) - K^2 \phi(x) = -K^2 V_{QN}^i \quad (3)$$

where

$$\phi(x) = \Psi(x, 0) - \Psi_{so}^i \quad (4)$$

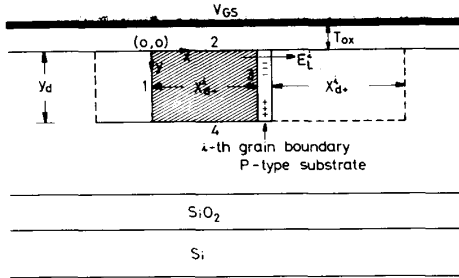


Fig. 1. The cross-sectional view of the i th grain in a TFT. The 2-D Poisson's equation is solved in the shaded region on the left/right side of the i th grain boundary.

$$K = \left[\frac{C_{ox}}{\epsilon_{si}} \cdot \frac{3}{y_d} \right]^{1/2} \quad (5)$$

and

$$V_{QN}^i = V_{GS} - V_{FB} - \Psi_{so}^i - \frac{qN_A y_d}{C_{ox}} \quad (6)$$

Solving (3) and using the following boundary conditions:

$$\phi(0) = 0 \quad \text{and} \quad \left. \frac{\partial \phi}{\partial x} \right|_{x=0} = 0 \quad (7)$$

one can easily obtain the solution as

$$\phi(x) = V_{QN}^i - V_{QN}^i \cosh(Kx). \quad (8)$$

Similarly, the potential distribution in the right side of the i th grain boundary can be easily calculated. Then, the electric field along the channel at the grain boundary is given by

$$KV_{QN}^i \sinh(Kx_{d\mp}^i) = \frac{Q_{GB\mp}^i}{2\epsilon_{si}} \mp E_L^i \quad (9)$$

where the symbol ($\mp$) means that the discussed region is in the left/right side of the i th grain boundary.

In general, the trapped charge density in the grain boundary depends on the distribution of the localized trapped states in the energy gap. Based upon previous work [9], the trap distribution can be well approximated by an effective trap state E_T , and the trapped charge density can be written as

$$Q_{GB\mp}^i = \frac{qN_{st}}{1 + \frac{1}{2} \exp \left[\frac{(E_T - E_F^i)|_{x=x_{d\mp}^i}}{k_B T} \right]} \quad (10)$$

where the position of the Fermi level relative to the trap level at the grain boundary can be related to the barrier height and the Fermi level in the undepleted channel by

$$(E_T - E_F^i)|_{x=x_{d\mp}^i} \approx (E_T - E_i) + q\Psi_{B\mp}^i - (E_F^i - E_i)|_{x=0}. \quad (11)$$

Note that the above relation neglects the variations of the quasi-Fermi level in the depletion region near the grain boundary. This approximation is valid for the TFT's operated in the turn-on region, where the population of traps is not sensitive to the variations of $(E_T - E_F^i)$ because all of the traps are filled by inversion carriers ($Q_{GB\mp}^i = qN_{st}$). It will be shown in Section III that, even in the saturation region, all of the traps along the current path are still filled by inversion carriers because the saturation behavior of TFT's is due to carrier velocity saturation and not due to pinchoff effect. When the TFT is operated in the subthreshold region, the grain boundary traps are not completely filled by inversion carriers and the effects of the drain bias on the trapped charges should not be overlooked. Under this condition, it is difficult to determine the trap population. However, the physical mechanism in the subthreshold region is not a focus point of our paper.

For a given grain size, there exist two possible conditions, depending on the lateral depletion width (x_d): (A) $x_d < L_g/2$ and (B) $x_d = L_g/2$. For case (A), only part of the grain is depleted of carriers and the inversion region exists on the left side of boundary 1, as shown in Fig. 1. Therefore, the gradual channel approximation is assumed to be valid in the inversion region, in which the normal component of the electric field is much larger than the lateral component, and the charge coupling between the gate and the grain boundary is small.

Combining (8) and (9), the i th grain barrier is obtained as

$$\begin{aligned} \Psi_{B\mp}^i &= |\phi(x_{d\mp}^i)| \\ &= \left[(V_{QN}^i)^2 + \left(\frac{Q_{GB\mp}^i}{2K\epsilon_{si}} \mp \frac{E_L^i}{K} \right)^2 \right]^{1/2} - V_{QN}^i \end{aligned} \quad (12)$$

where the effects of external biases on the i th grain barrier are revealed. From (12), the barrier height decreases with increasing gate bias, and the lateral electric field (E_L^i) emanating from the drain induces the potential barrier lowering on the left side and increasing on the right side.

Under a large gate voltage, all of the traps in the surface layer are filled by electrons, and the surface potential Ψ_{so}^i in V_{QN}^i can be approximated by $\phi_{s\text{inv}} + V_i$. The i th grain barrier in (12) can be simplified as

$$\begin{aligned} \Psi_{B\mp}^i &= \frac{y_{d\text{inv}}}{3} \frac{1}{C_{ox}(V_{GS} - V_{To} - V_i)} \\ &\quad \cdot \frac{(qN_{st} \mp \epsilon_{si} E_L^i)}{8\epsilon_{si}} \end{aligned} \quad (13)$$

and

$$V_{To} = V_{FB} + \phi_{s\text{inv}} + \frac{qN_A y_{d\text{inv}}}{C_{ox}} \quad (14)$$

where

$$\phi_{s\text{inv}} = 2 \frac{K_B T}{q} \ln \left(\frac{N_A}{n_i} \right)$$

for large-grain TFT's. From the above equation, it is clearly seen that the grain barrier is proportional to the oxide thickness and the depletion depth. Moreover, it is noted that (13) is different from the model proposed by Fossum and Ortiz-Conde [5] through the factor $y_{dinv}/3$ and the influence of the drain voltage. In [5], an arbitrary constant was introduced for the inversion-layer thickness in order to formulate the average density of inversion carriers.

If the gate bias is around the threshold voltage, the barrier height in (12) is fixed to Ψ_{B0}^i and is expressed as follows:

$$\Psi_{B0}^i = \left(\frac{Q_{GB}^i}{2K\epsilon_{si}} \mp \frac{E_L^i}{K} \right). \quad (15)$$

For case (B), the i th grain in the lateral direction is completely depleted (i.e., $x_d = L_g/2$), the electric field in the channel region is strongly perturbed by the charges at the grain boundary, and boundary line 4 can still be found somewhere in the bulk. In this case, the floating potential $\Psi(o, y_d)$ is not zero, but is a function of the bulk doping concentration, the grain size, and the trap states in the bulk grain boundary. As the band bending is toward the Si-SiO₂ interface, some induced carriers are captured by the traps in the grain boundaries. An additional gate voltage above V_{To} of a conventional MOSFET is required to support these extra charges in the traps. In this case, the surface band-bending ϕ_{so}^i is determined not only by the gate bias and the ionized charges in the bulk but also by the charge states of the traps at the grain boundaries. Its value is determined by

$$KV_{QN}^i \sinh(KL_g/2) = \frac{Q_{GB}^i}{2\epsilon_{si}} \mp E_L^i \quad (16)$$

in which the parameter of the Fermi level in Q_{GB}^i is given by

$$\begin{aligned} (E_F^i - E_i)|_{L_g/2} \\ \cong (E_T - E_i) + q\Psi_B^i - (q\phi_{so}^i - E_{fp} - qV_i) \end{aligned} \quad (17)$$

and

$$\Psi_B^i = V_{QN}^i [\cosh(KL_g/2) - 1] \quad (18)$$

where E_{fp} is the Fermi level in the bulk. From the theory of polycrystalline silicon film resistors [9], if N_A is less than a critical concentration N^* , the crystalline grain in the bulk is completely depleted in the lateral direction, and the hole concentration is less than N_A , i.e., $E_{fp} < K_B T \ln(N_A/n_i)$.

The threshold voltage (V_T) of a TFT with finite grain size is defined as the gate voltage at which the minimum surface potential is at the onset of strong inversion or the inversion carrier density at the surface is equal to the background doping concentration N_A . Since the position of the minimum surface potential is near the source, then ϕ_{so}^i and V_i in (16)–(18) are equal to ϕ_{sinv} and zero, re-

spectively. Rewriting (16), the threshold voltage V_T at the low drain bias can be obtained as

$$V_T = V_{To} + \frac{Q_{GB}|_{\phi_{sinv}}}{2\epsilon_{si}K \sinh(KL_g/2)} \quad (19)$$

where V_{To} for a fine-grain TFT is given by

$$V_{To} = V_{FB} + \Psi(o, y_{dinv}) + \phi_{sinv} + \frac{qN_A y_{dinv}}{C_{ox}} \quad (20)$$

and

$$\phi_{sinv} = \frac{K_B T}{q} \ln \left(\frac{N_A}{n_i} \right) + E_{fp}.$$

Note that the second term on the right-hand side of (19) is the extra gate voltage for filling the charges in the traps at the grain boundaries and has an exponential dependence on the grain size. Since $\Psi(o, y_{dinv})$ has a much weaker dependence on the grain size than that of the extra gate voltage, $\Psi(o, y_{dinv})$ can be simply lumped into the parameter V_{FB} for fine-grain TFT's.

III. I - V MODEL

In the channel, electrons across the barrier at the grain boundary must transport through the depletion region near the grain boundary and the inversion region far away from the grain boundaries. Since the emission over the barrier and the drift diffusion in the depleted and inversion regions are effectively in series, the one that offers high resistance determines the current. Several authors [10], [11] have combined these processes into a single theory. In this paper, the I - V characteristics of TFT's are based upon the interfacial-layer thermionic-diffusion model proposed by Wu and Ken [10] in which carrier transport mechanisms are described by thermionic-diffusion motion across the depletion region and quantum tunneling through the grain boundary.

In the inversion region of the i th grain, the current density is given by

$$J = qn(0, 0) \mu_n^i \frac{\delta V_i - V_{dp}^i}{L_g - W_T^i}. \quad (21)$$

In the depletion region of the i th grain boundary, the current density for any applied voltage is given by [10]

$$\begin{aligned} J = \frac{\nu_{Dn}^i \theta_n \nu_{Rn}}{\nu_{Dn}^i + \theta_n \nu_{Rn}} qn(0, 0) \exp(-\beta \Psi_{B-}^i) \\ \cdot [1 - \exp(-\beta V_{dp}^i)] \end{aligned} \quad (22)$$

where Ψ_{B-}^i is the grain barrier on the left side of the i th grain, as given in (12), in which the drain-induced grain barrier lowering effects are included. Moreover, for the small-bias limit ($V_{dp}^i < K_B T/q$), we obtain

$$J = \frac{\nu_{Dn}^i \theta_n \nu_{Rn}}{\nu_{Dn}^i + \theta_n \nu_{Rn}} qn(0, 0) \exp(-\beta \Psi_{B-}^i) \beta V_{dp}^i. \quad (23)$$

Under the strong inversion condition, the inversion carriers are almost confined in the surface layer. Integrating

(21) and (23) across the inversion layer, we obtain the total current, and the integrations of $qn(0, 0)$ can be replaced by the charge density induced in the surface layer $Q_n(V_i)$. From the above approximation, the current equation can be combined into a single expression as

$$I_{DS} \cong (\mu_n^i/F_i) W Q_n(V_i) (\delta V_i/L_g) \quad (24)$$

where

$$Q_n(V_i) = C_{ox}(V_{GS} - V_T - V_i) \quad (25)$$

$$F_i = \frac{\nu_{Dn}^i + \theta_n \nu_{Rn}}{\nu_{Dn}^i \theta_n \nu_{Rn}} \cdot \frac{\mu_n^i}{\beta L_g} \cdot \exp(\beta \Psi_{B-}^i) + (1 - W^i/L_g) \quad (26)$$

$$\begin{aligned} \nu_{Dn}^i = & (K_B T/q) \mu_n^i \left\{ \int_0^{x_{d-}^i} \exp[\beta V_{QN}^i (\cosh(Kx) - \cosh(Kx_{d-}^i))] dx \right. \\ & + \int_0^{x_{d+}^i} \exp[\beta V_{QN}^i (\cosh(Kx) - \cosh(Kx_{d+}^i))] dx \left. \right\}^{-1} \end{aligned} \quad (27)$$

in which V_{QN}^i is given in (6); Ψ_{so}^i is equal to $\phi_{sinv} + V_i$ at the strong-inversion mode; μ_n^i is the electron mobility in the surface layer. Due to the asperity of the polysilicon-SiO₂ interface, the surface-roughness scattering in poly-Si TFT's is more serious than that of single-Si MOSFET's. Therefore, it will introduce erroneous results for a wide range of gate biases if the mobility is taken to be a constant. The electron mobility including the effects of surface scattering and velocity saturation can be expressed as [12]

$$\mu_n^i = \frac{\mu_o}{1 + \theta(V_{GS} - V_T - V_i) + \frac{\mu_o}{\nu_{sl}} E_L^i + \xi} \quad (28)$$

where $\xi = 2\theta(qN_A y_{dinv}/C_{ox})$.

If the drain bias is small, the terms in F_i denoted with the superscript i are independent of the position, and the current I_{DS} can be easily integrated as

$$I_{DS} = (\mu_n/F) \frac{W}{L} C_{ox}[V_{GS} - V_T - V_{DS}/2] V_{DS} \quad (29)$$

For a large bias, the voltage drop across each grain is not equal, and transport mechanisms in each grain must be characterized by a large-signal model. The exact current-voltage characteristics can only be obtained by solving the $N_g - 1$ node equations for N_g grains. Due to higher complexity, it is desirable to simplify the formulation with some approximations: the average of the channel electric field $E_{L,ave}$ ($= \eta V_{DS}/L$) is used instead of the position-dependent parameter E_L^i in the evaluation of the barrier height Ψ_{B-}^i for $I-V$ formulation (24), where the parameter η is a factor used to consider the effect of nonlinear elec-

tric field along the surface channel [12]. Since the factor βV_{dp}^i in (23) is obtained by linearizing $[1 - \exp(-\beta V_{dp}^i)]$, which is multiplied with $\exp(-\beta \Psi_{B-}^i)$ in the general $I-V$ formulation (see (22)), the above approximation may reduce the errors introduced by extending the small-signal model in (23) to the large-signal model. Then, the parameters in F_i shown in (24) are only dependent on the potential along the surface channel. Multiplying both sides of (24) by L_g and integrating with respect to the potential along the surface, the drain current can be expressed as

$$I_{DS} = \frac{W}{L} \int_0^{V_{DS}} \frac{\mu_n}{F_i(V_i)} Q_n(V_i) dV_i \quad (30)$$

Noted that the threshold voltage V_T in $Q_n(V_i)$, as derived in the previous section, is valid for low drain-bias condition, and the variations of bulk depletion charges and trapped charges due to the drain voltage have been overlooked. The approximation used in V_T will affect the turn-on $I-V$ characteristics near the threshold voltage. However, the major drain-bias dependence of the derived $I-V$ characteristics is due to the exponential dependence of the grain barrier on the drain bias. Therefore, the effects of drain voltage on the threshold voltage can be overlooked without losing accuracy in the derivations of turn-on drain current at large gate bias.

As the drain bias increases, the electric field in the region near the drain is higher than the critical electric field (E_C); then the drift velocity of electrons approaches to a saturation value (ν_{sl}). The drain voltage needed to satisfy this condition is called the drain saturation voltage (V_{dsat}). The corresponding saturation drain current (I_{dsat}) can be obtained by using (30) with $V_{DS} = V_{dsat}$ and by (24) for the grain near the drain with $E_L^i = \delta V_i/L_g = E_C$ and $V_i = V_{dsat}$. Equating these two saturation drain currents, the value of V_{dsat} can be determined. In the saturation region, the density of free carriers in (30) can be expressed as

$$Q_n(V_i) = C_{ox}[V_{GS} - V_T - V_{dsat}] \quad \text{for } V_i \geq V_{dsat} \quad (31)$$

and the effective electron velocity is a constant, which is the saturation velocity (ν_{sl}) in series with the effective velocity across the depletion region and the grain boundary. It should be noted that the drain current does not level off beyond the saturation point, but shows the exponential dependence on the drain voltage due to the DIGBL effects. Moreover, the carriers in the saturation region are not pinched off, and all the traps in the carrier flow path are still filled by electrons. Thus, the modulation of the trapped charges by the drain voltage can be neglected without introducing large errors.

IV. RESULTS AND DISCUSSIONS

A. Theoretical Analysis

In order to demonstrate the physical pictures from our previous derivations, the set of physical parameters listed in Table I is used unless mentioned otherwise. From (19),

TABLE I
THE PARAMETERS USED FOR SIMULATION

N_{st} (10^{12} cm $^{-2}$)	2.69
$E_T - E_i$ (eV)	-0.08
L_g (10^{-8} cm)	2090
V_{T0} (V)	0.81
$\theta_n \nu_{Rn}$ (10^6 cm/s)	0.34
μ_0 (cm ^{2} /V-s)	90.0
θ	0.857
E_C (10^4 V/cm)	4.0
ν_{sl} (10^6 cm/s)	8.0

the effects of grain size on the threshold voltage are calculated and shown in Fig. 2. It shows that the smaller the grain size is, the larger the threshold voltage will be. Moreover, for a TFT with larger grain size, the threshold voltage (V_T) will approach to that of a single-Si MOSFET. From (12) and (18), the variations of the grain barrier with respect to the gate bias for different grain sizes are calculated and shown in Fig. 3. It shows that the potential barrier height increases with increasing the gate bias at first, reaches a peak value at the onset of strong inversion ($V_{GS} = V_T$), and then decreases. Since some induced carriers are captured by the traps, the barrier height increases initially with increasing gate bias. As the gate bias is further increased, all of the traps are filled, and the total trapped charges remain the same. But, the lateral depletion width (x_d) decreases, so the barrier height rolls off. Moreover, it shows that the smaller the grain size is, the lower the barrier height will be. This feature is due to the fact that ϕ_{sinv} decreases with decreasing grain size.

The theoretical curves showing the effects of trapping density and grain size on the conductance (I_{DS}/V_{DS}) and the effective mobility (μ_n/F) are shown in Figs. 4 and 5, respectively, in which the same parameter values except the trapping density are used in order to easily compare the characteristics of TFT's affected by the variations of trapping density. The effective mobility versus the gate voltage can be generally divided into two regions, as shown in Fig. 4. The effective mobility first monotonically increases with the gate voltage, and then decreases gradually. At low gate voltage, the current flow is limited by the depletion region. The monotonic increase of the effective mobility is due to the fact that the potential barrier decreases with increasing the gate voltage, as discussed in the previous section. When the potential barrier decreases to a value smaller than the thermal voltage ($K_B T/q$), the current flow is limited by the inversion region in which the surface roughness scattering causes the effective mobility decrease. For the case of higher trapping density, the potential barrier is still much larger than the thermal voltage under the gate bias range, as shown

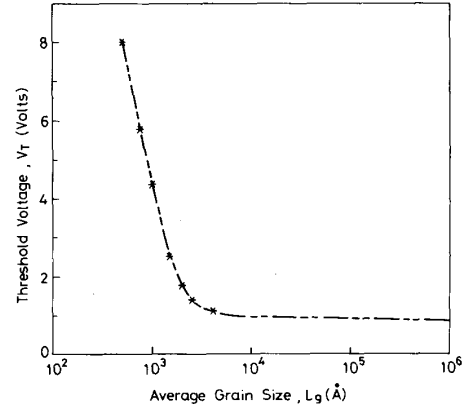


Fig. 2. The calculated threshold voltage (V_T) with respect to the grain size. The parameters used for simulation except the grain size are listed in Table I.

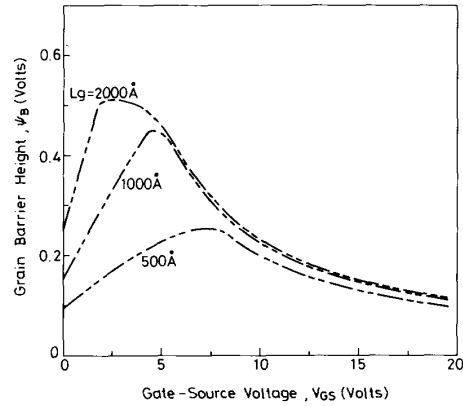


Fig. 3. The calculated barrier height versus the gate bias for different grain sizes. The parameters used for simulation except the grain size are listed in Table I.

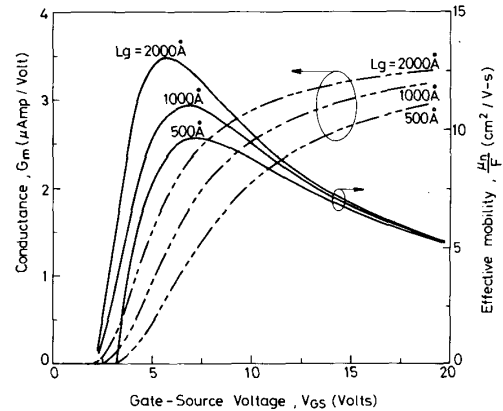


Fig. 4. The calculated conductance (dashed line) and effective mobility (solid line) versus the gate voltage for different grain sizes. The parameters used except the trapping density ($N_{st} = 8.0 \times 10^{11}$ cm $^{-2}$) are the same as those in Table I.

in Fig. 3, and thus the current is only limited by the grain boundary and its depletion region. Although the difference in the effective mobility for the grain sizes smaller

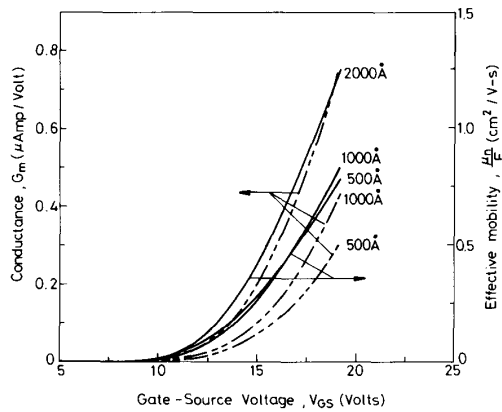


Fig. 5. The calculated conductance (dashed line) and effective mobility (solid line) versus the gate voltage for different grain sizes. The parameters used are the same as those in Table I.

than 1000 Å is small, the difference in the conductance is large, as shown in Fig. 5. This phenomenon is mainly due to the fact that the threshold voltage (V_T) is strongly dependent on the grain size, as shown in Fig. 2.

B. Experimental Results and Theoretical Comparisons

In order to test the validity of the developed I - V model, n-channel enhancement poly-Si TFT's were fabricated. A small-grain poly-Si film of 550 nm was deposited onto a 600-nm SiO_2 layer thermally grown on p-type bulk Si by the LPCVD method at 625°C. The LPCVD poly-Si was then implanted using boron ions at 60 keV with a dose of $5 \times 10^{12} \text{ cm}^{-2}$. After being patterned into individual devices, a 98-nm gate oxide film was grown by dry oxidation, and then another LPCVD poly-Si film of 550 nm was deposited. The source, the drain, and the poly-Si gate were simultaneously implanted using arsenic ions at 180 keV with a dose of $4 \times 10^{15} \text{ cm}^{-2}$. The average channel concentration is estimated to be about $1.0 \times 10^{17} \text{ cm}^{-3}$.

The effective channel length is determined by the drain current ratio of two different channel-length devices and is shown in the Appendix. The parameter extraction procedure is described as follows. Invoking (13), the parameters N_{st} and V_{T0} can be estimated by linear extrapolation on the plot of $1/\Psi_B$ versus V_{GS} at the low drain bias condition. The grain size L_g and the effective trapped level E_T can be estimated by comparing the experimental barrier-height data versus the applied low gate voltage. From the values of V_{T0} and L_g , the effective surface fixed charge density Q_{ss} can be determined, and the order of μ_0 can be estimated. Then, the values of μ_0 , θ , and $\theta_n \nu_{Rn}$ are determined by comparing the experimental drain current versus the applied gate voltage at low drain voltage. The remaining parameters, η and E_C , are extracted at large drain voltage by comparing the drain current versus the drain voltage. Finally, all parameters are slightly adjusted by the nonlinear optimizer [13] to get the best I - V fittings. Table I lists the parameters used in our simulations.

Fig. 6 shows the Arrhenius plots of the measured drain current versus the inverse of temperature for different gate

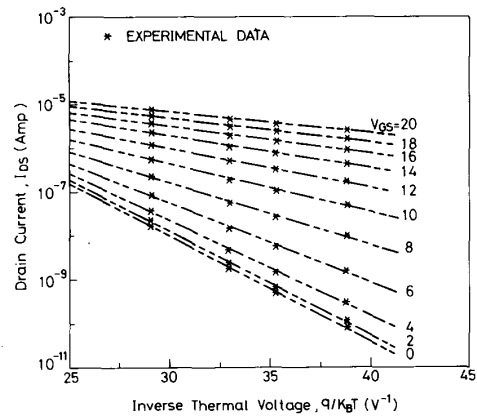


Fig. 6. The Arrhenius plot of the measured I_{DS} versus the inverse thermal voltage ($q/K_B T$) for different gate biases and $V_{DS} = 0.5 \text{ V}$.

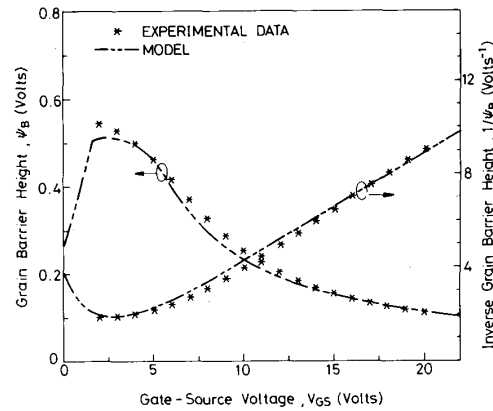


Fig. 7. The experimental and simulated (inverse) potential barriers versus the gate bias.

biases and a drain voltage of 0.5 V. The strong dependence of the drain current on temperature is mainly due to the formation of the potential barrier along the flow path of carriers, and the activation energy or the potential barrier height can be deduced from Fig. 6. Fig. 7 illustrates the measured potential barrier height with respect to the applied gate voltage and its comparisons with the calculated results. Moreover, Fig. 7 also shows the linearity on the plot of $1/\Psi_B$ versus V_{GS} under the large gate bias condition. From Fig. 7, it is clearly seen that the agreement between the measured barrier height and the theoretical results is good for $V_{GS} > V_T$. However, the discrepancy for the bias below the threshold voltage ($V_T = 1.68$) is mainly due to the fact that the measured I_{DS} is contributed by the subthreshold current or the anomalous leakage current [14]. The I - V characteristics of TFT's with long ($L = 7.5 \mu\text{m}$) and short ($L = 2.5 \mu\text{m}$) channel length are investigated. Fig. 8 shows the effective mobility (μ_n/F) with respect to the gate voltage at low drain voltage. The increase of the effective mobility with respect to the gate voltage means that the current is limited by the grain boundary and its nearby depletion region, as

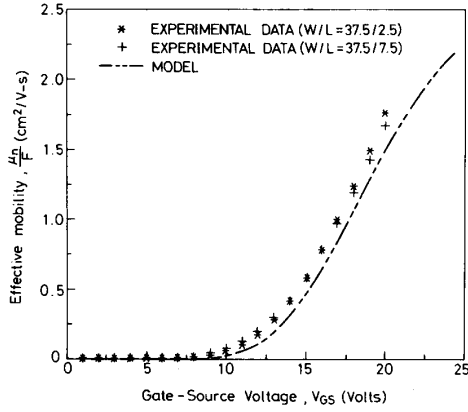


Fig. 8. Experimental and simulated effective mobilities versus the gate bias.

discussed previously. Fig. 9 shows the experimental and calculated I - V characteristics for different gate biases. Good agreement between the calculated results and the experimental data for long- and short-channel-length TFT's has been obtained. The value of the maximum electron mobility (μ_0) in the surface channel is only $90 \text{ cm}^2/\text{V-s}$. This may be due to higher channel doping N_A ($= 1.0 \times 10^{17} \text{ cm}^{-3}$) as well as fixed charge density Q_{ss} ($= 8.2 \times 10^{11} \text{ cm}^{-2}$). The parameter θ used in our simulation is about an order larger than that of single-Si MOSFET's [12], which is attributed to the effect of surface roughness. The transmission coefficient across the grain boundary (θ_n) is much less than unity, which means that the scattering of electrons in the grain boundary cannot be neglected. The average grain size used in our simulation is $2090 \text{ \AA}$ and is within the order of the data reported in [15], in which the grain size near the top of the LPCVD $0.47\text{-}\mu\text{m}$ poly-Si film deposited at 620°C is approximately $0.15\text{--}0.2 \text{ }\mu\text{m}$.

It is noted that the normalized current ($I_{DS} * L/W$) of a short-channel TFT is larger than that of a long-channel device. Moreover, the drain current under large drain bias has the exponential dependence on the drain voltage and does not level off above the saturation point, as marked by the dots in Fig. 9. These characteristics are quite different from those of single-Si MOSFET's. Although the effective carrier velocity and carrier charge density are constant in the saturation region, the grain barrier in the surface layer is modulated by the drain voltage. Therefore, extra carriers are injected from the lowered barrier side and introduce extra current flow.

V. CONCLUSIONS

In this paper, a quasi-two-dimensional analytical method has been developed to calculate the grain barrier height of a polysilicon TFT, and it includes the effects of charge coupling between the gate and the grain boundary as well as drain-induced grain barrier lowering. Based upon the developed grain barrier model, the threshold voltage has been derived in terms of grain size, trapped

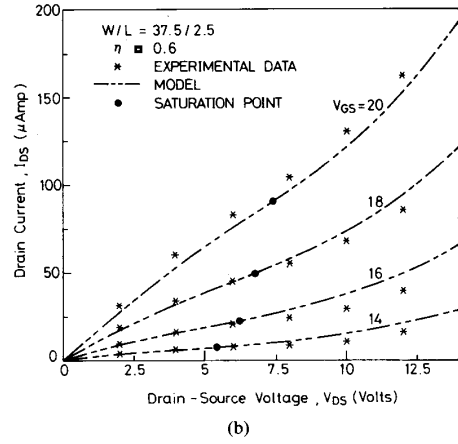
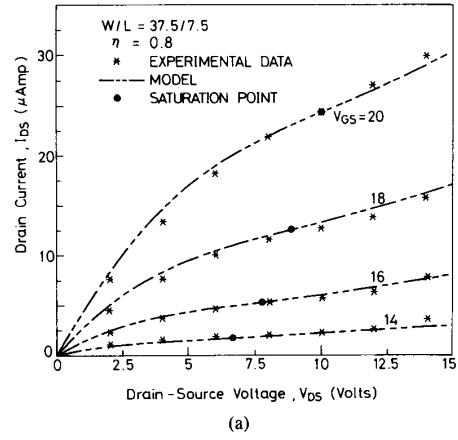


Fig. 9. The simulated and experimental output I - V characteristics: (a) $W/L = 37.5/7.5$; (b) $W/L = 37.5/2.5$.

charge density, and substrate doping density. Moreover, the I - V model is developed by using the interfacial-layer thermionic-diffusion model. The attractive features of the developed models are: 1) the threshold voltage of a TFT has an exponential dependence on the grain size (the smaller the grain size is, the larger the threshold voltage will be); 2) drain bias will produce asymmetric grain barriers and introduces more carrier injection from the lowered barrier side, which results in the exponential dependence of the drain current on the large drain voltage. From comparisons between experimental devices and calculated results, the developed I - V model is quite successful in explaining the experimental observations.

APPENDIX

THE DETERMINATION OF THE CHANNEL LENGTH

Let L_{mi} and ΔL_i denote the mask and the bias length of the i th device. Based upon the current equation (29), the current ratio of two devices with different channel lengths can be expressed as

$$\frac{L_{DS1}}{L_{DS2}} = g_{12} = \frac{L_{m2} - \Delta L_2}{L_{m1} - \Delta L_1} \quad (\text{A1})$$

because the other parameters are independent of the channel length. If the mask length L_{m2} is much larger than the difference of two bias lengths (i.e., $L_{m2} \gg \Delta L_1 - \Delta L_2$), the effective length of two devices is obtained by

$$L_{\text{eff}1} = L_{m1} - \Delta L_1 \quad (\text{A2})$$

where

$$\Delta L_1 = \frac{g_{12}L_{m1} - L_{m2}}{g_{12} - 1} \quad (\text{A3})$$

Then, another channel length of device 3 is given as

$$L_{\text{eff}3} = L_{\text{eff}1} * g_{13} \quad (\text{A4})$$

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Pole-Shang Lin photograph and biography not available at the time of publication.

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