



Reliability of Passivated P-type Polycrystalline Silicon Thin Film Transistors

D.Z. Peng ^{a,*}, P.S. Shin ^a, T.C. Chang ^b, C.Y. Chang ^a

^a*Institute of Electronics, National Chiao Tung University, Taiwan*

^b*Department of Physics, National Sun Yat-Sen University, Taiwan*

Abstract

We have used NH_3 , N_2O and N_2 to passivate the traps in the grain boundaries of the p-type polycrystalline silicon thin film transistors (p-type poly-Si TFTs). Two different stress conditions, drain voltage V_d of -15V and -30V, have been applied to the poly-Si TFTs respectively while the gate voltage V_g were kept at -15V for both conditions and the stress time were 10 minutes at room temperature for all samples. The comparisons of I-V characteristics after stress with and without plasma passivations have been made, and the results indicated that the reliability will become worse for poly-Si TFTs after plasma passivations. © 2000 Elsevier Science Ltd. All rights reserved.

1. Introduction

Polycrystalline silicon thin film transistors are of interests for their widely applications in active matrix liquid crystal displays (AMLCDs)[1] and some memory devices such as dynamic random access memories (DRAMs)[2]. In order to obtain better device performance, plasma passivation is usually used to passivate the traps in the grain boundaries[3]. It is known that H_2 plasma treatment will lead to tie up the hydrogen with the grain boundary dangling bonds, and therefore dramatically promote the device performances.

Unfortunately, the hydrogen passivation suffer a poor hot-carrier endurance because of the weak Si-H bond[4]. F. S. Wang et al. compared the H_2 and the NH_3 passivated n-type TFTs[5] and showed that H_2 passivation resulted in a lower hot carrier endurance than NH_3 passivation. On the other hand,

Y. S. Lee found that the hot carrier endurance of N_2 plasma treatment is better than that of the NH_3 plasma treatment for n-type TFTs[6].

In this experiment, we have used NH_3 , N_2 , and N_2O to passivate the traps in the grain boundaries of the p-type TFTs, and we have applied two different stress conditions to accelerate the degradation of device performance. The results showed that the passivated poly-Si TFTs suffer lower stress endurance than unpassivated poly-Si TFTs. The p-type poly-Si TFTs after NH_3 , N_2 , and N_2O plasma passivation show little differences after the stress in this experiment which are not seen in the previous results[5,6] for n-type TFTs.

2. Experiments

2.1. Device fabrication

* Corresponding author.

Email address: u8711817@cc.nctu.edu.tw

A 500nm thermally grown silicon-dioxide (SiO_2) was used as the starting substrate. Undoped amorphous silicon (a-Si) layers of thickness 100nm were deposited by low pressure chemical vapor deposition (LPCVD) on the oxide by pyrolysis of disilane (Si_2H_6) at 460 °C and the deposition pressure was 120 mTorr. The a-Si film was recrystallized to poly-Si film in N_2 ambient for 24 hours by furnace annealing. The crystallized poly-Si was employed as the channel layer with the grain size of about 1 μm . After defining the active islands, a 40nm thick SiO_2 was thermally grown by dry oxidation. Another 300nm poly-Si film was deposited at 620 °C in the LPCVD system and patterned to be the gates of the devices. The source, drain, and gate regions were implanted by Boron for p-channel TFTs. After ion implantation, these samples were annealed in N_2 ambient at 900 °C to activate the dopants. A 200nm-thick passivation oxide was deposited by PECVD at 300 °C. The contact holes were opened and a 500nm aluminum layer were deposited by thermal evaporation system. The aluminum layer was then patterned as the metal pad for measurement. Three different gas sources of NH_3 , N_2O and N_2 were used to passivate the p-type poly-Si TFTs in the PECVD system at 300 °C, and the passivation time was 2 hours.

2.2. Stress conditions

Two different stress conditions were employed to the p-type poly-Si TFTs both for as fabricated devices and the devices after plasma passivations. The stress time is 10 minutes at room temperature for all samples.

- Condition 1: $V_g = -15\text{V}$ and $V_d = -15\text{V}$, $W/L = 50\mu\text{m}/5\mu\text{m}$
- Condition 2: $V_g = -15\text{V}$ and $V_d = -30\text{V}$, $W/L = 10\mu\text{m}/5\mu\text{m}$

3. Result and discussion

Fig. 1 compares the I_d - V_g characteristics for as fabricated devices and those after plasma passivations of NH_3 , N_2O , and N_2 , respectively. It can be seen that after plasma treatment, the turn on current, subthreshold swing, threshold voltage and leakage current ($V_g > 0$ for p-type TFTs) are significantly improved, which is attributed to the formation of Si-H and/or Si-N bonds in the poly-Si channel layer and Si/ SiO_2 interface after plasma

passivations[3,7], thereby reducing the dangling bonds and hence the trap state density (N_t) in the poly-Si layer and Si/ SiO_2 interface.

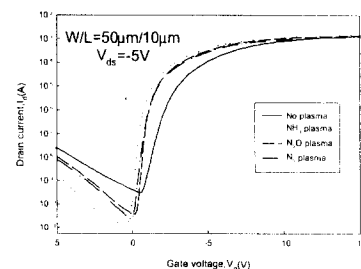


Fig. 1 The transfer curves of drain current, I_d versus the gate voltage, V_g for p-type TFTs with and without plasma treatment

Fig. 2~Fig. 5 show the I_d - V_g characteristics before and after stress condition 1 for unpassivated devices, NH_3 , N_2O , and N_2 passivated devices, respectively. From Fig. 2, we can find that the device without passivation shows little change except for the reduced leakage current, while from Fig. 3~Fig. 5 for passivated TFTs, it can be seen that after stress, the performances become a little poor, i.e., subthreshold swing increases, threshold voltage shift and the field effect mobility degrades. However, the on/off current ratio, which is defined as the maximum current divided by the minimum current at $V_d = -5\text{V}$, is increased because of the reduced leakage current. The degradations after stress condition 1 for passivated devices are almost the same in spite of their passivation sources, and the variations of some parameters after stress for unpassivated and passivated devices are listed in table 1. Note that the parameters were all characterized in linear region ($V_d = -0.1\text{V}$), except for the minimum drain current, which is calculated at $V_d = -5\text{V}$.

Fig. 6~Fig. 9 show the I_d - V_g characteristics before and after stress condition 2 for unpassivated, NH_3 , N_2O , and N_2 passivated devices, respectively. The unpassivated poly-Si TFT after stress behaved like stress condition 1, i.e., only reducing the leakage current. Fig. 7~Fig. 9 for passivated TFTs show, however, more severe degradations than those observed in stress condition 1, including the dramatic degradation of subthreshold swing and

large shift of threshold voltage. In opposite to the stress condition 1 for passivated devices, the on/off current ratio under stress condition 2 now reduced which is due to the increase of the leakage current. The variations of parameters are summarized in table 2. All parameters were extracted in linear region, except for $I_{\min}$ determined at $V_d = -5V$.

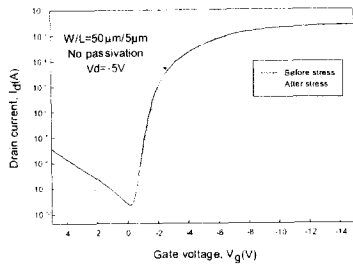


Fig. 2 The transfer curves of I_d - V_g before and after stress condition 1 for unpassivated p-type poly-Si TFT

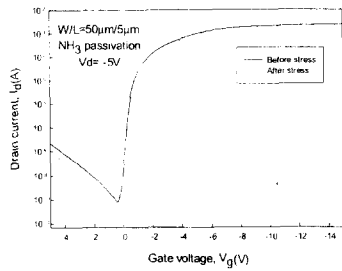


Fig. 3 The transfer curves of I_d - V_g before and after stress condition 1 for NH_3 passivation

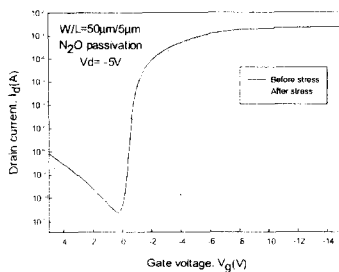


Fig. 4 The transfer curves of I_d - V_g before and after stress condition 1 for N_2O passivation

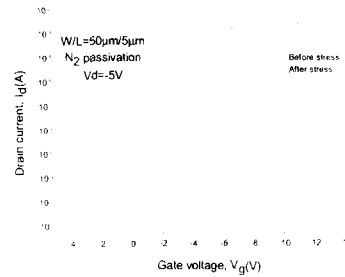


Fig. 5 The transfer curves of I_d - V_g before and after stress condition 1 for N_2 passivated p-type poly-Si TFT

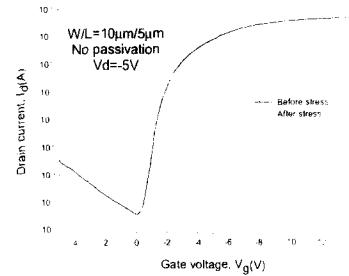


Fig. 6 The transfer curves of I_d - V_g before and after stress condition 2 for unpassivated poly-Si TFT

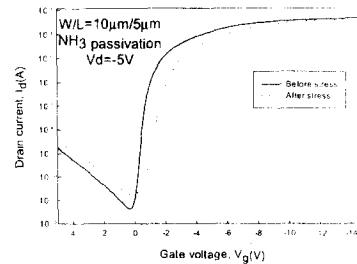


Fig. 7 The transfer curves of I_d - V_g before and after stress condition 2 for NH_3 passivation

In table 1 the device performance without plasma treatment after stress condition 1 shows only a reduced off current, and those with plasma treatment after stress condition 1 have a little changes in addition to the reduced off current. One reason for this is that stress condition 1 causes electron traps in the oxide for the unpassivated device near the drain side[8], and both the electron trap in the oxide and breaking of the Si-H, Si-N bonds in the poly-Si layer and/or poly-Si/SiO₂

interface for the passivated ones, which can be seen from the variations of effective trap state density (N_t) extracted from slope of $\ln [I_d/(V_g - V_{fb})]$ vs $(V_g - V_{fb})^{-2}$ characteristic[9] as shown in Fig. 10 and Fig. 11 for unpassivated, NH_3 passivated devices, respectively before and after stress condition 1. V_{fb} denotes the flat band voltage.

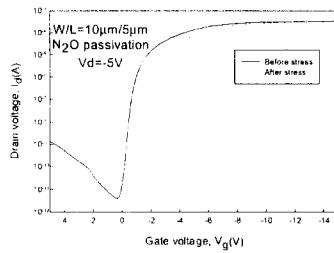


Fig. 8 The transfer curves of I_d - V_g before and after stress condition 2 for N_2O passivated p-type poly-Si TFT

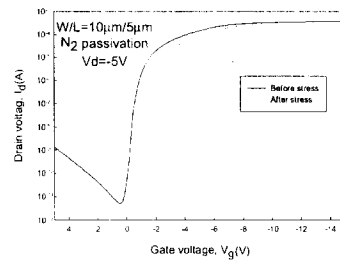


Fig. 9 The transfer curves of I_d - V_g before and after stress condition 2 for N_2 passivated p-type poly-Si TFT

The trapped electron in the oxide near the drain side will reduced the longitude electric field in the poly-Si film near drain when device is operated in the off state ($V_g > 0$, $V_d < 0$), and therefore the off current is reduced for the unpassivated device[8]. As mentioned above, both trapped electron and breaking of Si-H, Si-N bonds exist in the poly-Si layer and/or poly-Si/ SiO_2 interface, the dominant term is, however, the electron trap so that the off current is still reduced accompanied with a little change of the turn on characteristics for the passivated devices. In table 2 for the passivated devices, due to the large voltage applied to the gate and drain, the breaking of Si-H, Si-N was the dominant term under stress condition 2, resulting in increased donor-type trap state density[10], which can be verified in Fig. 12 with

large increase of N_t after stress condition 2. This is the consequence of the significant change of device performance. Nevertheless, unpassivated devices show little change as with those in stress condition 1. The Si-H, Si-N bonds originally used to passivate the dangling bonds of poly-Si layer and/or poly-Si/ SiO_2 interface were broken again after the stress, so that the reliability of passivated device is an important issue for poly-Si TFTs.

Table 1

Variations of parameters after stress: $V_d = V_g = -15\text{V}$. μ_{EF} , S.S, I_{min} , V_{th} are the field effect mobility, subthreshold swing, minimum drain current and the threshold voltage, respectively.

Passivation	$\Delta \mu_{EF} / \mu_{EF}$	$\Delta \text{S.S} / \text{S.S}$	$\Delta I_{min} / I_{min}$	$\Delta V_{th} (V)$
-----	-0.01	0.02	-0.53	0.02
NH_3	-0.05	0.26	-0.76	-0.38
N_2O	-0.02	0.26	-0.63	-0.34
N_2	-0.02	0.09	-0.62	-0.26

Table 2

Variations of parameters after stress: $V_d = 2V_g = -30\text{V}$. μ_{EF} , S.S, I_{min} , V_{th} are the field effect mobility, subthreshold swing, minimum drain current and the threshold voltage, respectively.

Passivation	$\Delta \mu_{EF} / \mu_{EF}$	$\Delta \text{S.S} / \text{S.S}$	$\Delta I_{min} / I_{min}$	$\Delta V_{th} (V)$
-----	~ 0	~ 0	-0.54	~ 0
NH_3	-0.18	0.85	3.25	-1.23
N_2O	-0.14	0.47	4.50	-1.15
N_2	-0.16	1.00	14.40	-1.09

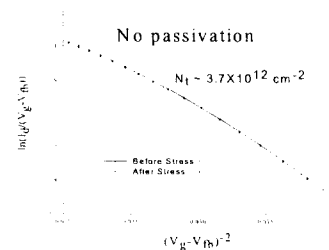


Fig. 10 Slope of plot used to determine the value of trap state density, N_t for unpassivated TFT before and after stress condition 1.

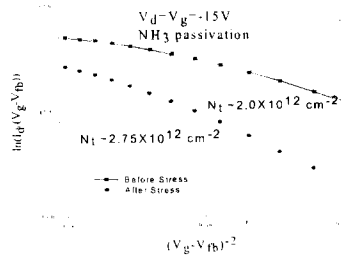


Fig. 11 Slope of plot used to determine the value of trap state density, N_t for NH_3 passivated TFT before and after stress condition 1.

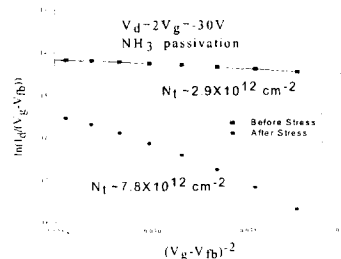


Fig. 12 Slope of plot used to determine the value of trap state density, N_t for NH_3 passivated TFT before and after stress condition 2.

4. Conclusion

Reliability of unpassivated, NH_3 , N_2O and N_2 passivated p-type poly-Si TFTs was studied after two stress conditions. Under stress condition 1, $V_g = V_d = -15\text{V}$, the unpassivated devices show almost no change with its turn on characteristics but with reduced leakage current, while for passivated devices there is a little change with its turn on curve in addition to the reduced leakage current. At stress condition 2, $V_d = 2V_g = -30\text{V}$, the performance of passivated devices become poorer compared with that in stress condition 1, and the change of I_d - V_g characteristics after stress condition 2 for unpassivated devices is the same as in stress condition 1.

The results indicate that there are electron traps in the gate oxide for unpassivated devices, the extracted N_t ($\sim 3.7 \times 10^{12} \text{ cm}^{-2}$) shows no difference

before and after stress. Nevertheless, in addition to the electron traps, there are generations of N_t for passivated devices especially larger for higher drain stressed, and the ΔN_t after stress condition 1 and 2 are $0.75 \times 10^{12} \text{ cm}^{-2}$ and $5.8 \times 10^{12} \text{ cm}^{-2}$, respectively, for NH_3 passivation. So we can conclude that after plasma passivation the p-type poly-Si TFTs show poorer reliability than unpassivated devices in spite of which one of the three passivation sources is chosen.

References

- [1] S. Morozumi, K. Oguchi, S. Yazawa, T. Kodaira, H. Ohshima, and T. Mano, SID Dig., 1983, p. 156.
- [2] S. D. S. Malhi, H. Shichijo, S. K. Banerjee, R. Sundaresan, M. Elahy, G. P. Polack, W. F. Richardson, A. H. Shah, L. R. Hite, R. H. Womack, P. K. Chatterjee, and H. W. Lam, IEEE Trans. Electron Devices, 1985, vol. 32, No. 2, pp. 258–281.
- [3] T. I. Kamins, and P. J. Marcoux, IEEE Electron Device Lett, 1980, vol. 1, p. 159
- [4] S. Banerjee, R. Sundaresan, H. Schichijo, and S. Malhi, IEEE Trans. Electron Devices, 1988, vol. 35, pp. 152–157
- [5] F. S. Wang, M. J. Tsai, and H. C. Cheng, IEEE Electron Device Lett., 1995, vol. 16, No. 11, pp. 503–505.
- [6] Y. S. Lee, H. Y. Lin, T. F. Lei, T. Y. Huang, T. C. Chang and C. Y. Chang, Jpn. J. Appl. Phys., 1998, vol. 37, No. 7, pp. 3900–3903.
- [7] J. H. Kim, E. Y. Oh, B. C. Ahn, and D. Kim, Appl. Phys. Lett., 1994, vol. 64, No. 6, pp. 775–776.
- [8] J.Y. Lee, C.H. Han; C.K. Kim, Tech Dig IEDM, 1995, pp.523–526.
- [9] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Ride, J. Appl. Phys, 1982, vol. 53, No. 2, pp. 1193–1202.
- [10] Rodder, M, IEEE Electron Device Lett, 1990, vol 118, pp. 346–348.