

對以智財單元為基系統晶片設計之驗證與測試技術開發研究

Verification and Testing Technology Exploitation for IP-Based SOC Design

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一、中文摘要

以系統晶片來實現複雜的系統已成為積體電路設計的主要趨勢。系統晶片的設計一方面要利用強大計算機輔助設計整合多個智財(IP)單元於單一的系統晶片上，另一方面要驗證設計結果以符合系統要求。為達成後者目的需要有強大有效之驗證測試系統。本研究團隊基於多年研究積體電路驗證測試技術的經驗提出此計畫以開發出完整的系統晶片驗證測試技術。

計劃分成四子計劃，分三年完成。分別為：(1)於組織探索階段互動之系統階層驗證技術；(2)以智財為基系統晶片設計之功能驗證技術研究；(3)以智財為基系統晶片設計之測試技術研究；與(4)系統晶片矽晶偵錯之良率提昇。分別於系統階層驗證、RTL 階層驗證、IP 單元測試、與元件偵錯四層面上發展驗證、測試、偵錯與良率提昇技術，以減少再設計週期。藉由探討此四個部分的驗證技術及相互間的分工整合建構成一套具實用性的系統晶片驗證測試偵錯技術。

關鍵詞：系統晶片、驗證、測試、偵錯、超大型積體電路/計算機輔助設計、良率

Abstract

To use an SOC (System-On-a-Chip) realize a complex system has become the main trend for today's IC design. To design an SOC, in one hand, it needs to have a powerful CAD system to incorporate many

IP's into one single chip; in the other hand, it needs to verify the designed system and test the finally fabricated chip to guarantee its proper function and performance. To achieve the latter goal, it needs to have a powerful and effective verification, testing and debug system. In view of this, this integrated joint project is proposed to investigate the verification, testing and diagnostic technology for the SOC design.

The project, to be carried out in three year period, has four sub-projects, which are : (1) system-level verification interacting with architecture exploration; (2) Functional verification techniques for IP-based SOC design; (3) Testing technology development for IP-based SOC design; and (4) SOC silicon diagnostics and yield improvement. It is dedicated to investigate the verification, testing and debug techniques at four levels, i.e., system level, RTL level, IP-level and silicon wafer debug of SOC design. The final aim is to develop a complete and practical verification and testing system for SOC design.

Keywords: SOC, Verification, Testing, Diagnosis, VLSI/CAD, Yield

二、緣由與目的

以系統晶片(System-on-Chip)來實現複雜的系統已成為積體電路設計的主要趨勢。系統晶片的設計一方面要整合多個智財(IP)單元於單一的系統晶片上，另一方面要驗證設計結果以符合系統要求。合

成智財單元與整合系統晶片的過程繁複已屬不易，而要確認該系統晶片製造完成後，是否能正確地運作則是更大的挑戰。目前學術及產業界大多投入於系統晶片的開發設計上，對於系統晶片的驗證測試技術則著墨不多。鑑於此，本研究團隊提出此計畫以開發出完整的系統晶片驗證測試技術。

系統晶片設計通常採用由上而下的流程，分為 System-Level Design，RTL-Level Design, Gate-Level Design 以及 Manufacturing，在每一層次設計均產生 intermediate 設計結果供下一層次之設計使用。在每進入下一個層次之前，必須先確認設計結果之正確性與其之可測試性。我們所提出一套結合設計流程的驗證程序，分階段地：即 System level, RTL-level, Gate level 及 Manufacturing level 完成系統晶片的驗證工作及產生測試偵錯圖樣(test and diagnostic patterns)。

第一階段主要是由第一子計畫執行，其主要工作是成本評估、效能模型、軟硬體共模擬。此計畫首先就耗電功率、面積、延遲時間三項因素來評估系統之組織成本。根據與系統組織配置的設計階段互動，一方面驗證該組織是否符合系統要求、一方面提供組織配置的設計參考。此步驟完成後，再在效能抽象階層上模擬候選組織。在此階層的模型不強調實際的資料值而僅考慮系統內的資料流動。因此，由於模型複雜度的簡化縮短模擬時間。而設計者依據時間性效能的模擬結果驗證候選組織並進而改善設計。完成此二步驟後，軟硬體共模擬開始就包含軟、硬體元件的異質組織實施模擬以驗證系統晶片行為結果。至此，系統階層驗證便告完成。此時將再進行下列階段 RT-level 之驗證。

第二階段主要是由第二子計畫執行。第二子計畫擬對不同的 IPs，特別是內嵌式處理器，DSP IPs 及匯流排，發展出不同的驗證演算法，然後建構一驗證系統將所發展之演算法納入，以實地的驗證一些上述 IPs，另外本計畫亦擬研究一些

System level 與 RTL level 設計間的同等問題(equivalence checking)，以保證當一 SOC 設計自 System level 轉至 RTL level 時無誤。

第三階段主要是由第三子計畫執行。於 SOC 設計過程中，除各層次之設計驗證外，為保證系統晶片製造出來時，無因製程缺陷等因素而發生不能工作情況，必須加入可測試性設計之考慮，並對各 IP 產生其測試與偵錯圖樣。晶片測試，長久以來即是一困難問題。於系統晶片設計中，由於晶片之規模是更大而複雜，且其中許多 IP，皆是由不同公司或設計者提供，所設計出來之晶片測試問題更是嚴重。又未來之系統晶片，必是屬混模信號(mixed-mode signal)，其製造技術亦必是以深次微米為主之技術，其信號傳輸是以奈秒(nano-seconds)(甚至以上)為單位。對於此種晶片，有一些新的現象，如：信號於 interconnection wires 傳輸所花費時間將超過於 MOSFET 電晶體傳輸所花費時間，interconnection wires 間之信號干擾現象嚴重，MOSFET 漏電流增大等，晶片測試需要有新的考量。

故第三子計畫：擬在下列三方向對 SOC 晶片測試之諸問題，作一研究：(1) 數位與類比 IP 之測試與驗證；(2) 深次微米連接線之測試；(3) 以統計方法研究深次微米 VLSI 測試。其中第一項係於 gate 或 circuit level 對各類 IP 研究其測試方法，特別是採用自我測試之方式；第二項係針對未來 SOC 必是將許多 IPs 用連接線連接，此連接線會因次微米而有一些如上所述現象，其測試值得研究；第三項係因深次微米晶片，其功能受製程參數影響甚大，處理測試問題已不可循往常固定值之測試觀念，而必須以統計方式處理。

於第四晶片製造階段，由於製程初始之 immature tuning，所生產之晶片良率必低，或於晶片測試時發現晶片不符規格，必須經由晶片偵錯，甚或設計偵錯，發現原因，而提升晶片生產良率。此時甚或需全面檢討晶片設計，以求達到最符經濟效率的測試與晶圓良率，此階段工作係

由第四子計畫執行。其於矽晶片製造完成後，就其測試資料，即 wafer map，尋求設計、測試與製造流程之缺失，並藉統計理論分析良率以增進晶片良率與提升晶片品質。另外亦欲以系統分析方式研究系統晶片之整個設計、測試與製造的流程，以改進晶片良率與提升晶片品質。最後此子計畫更擬研究系統晶片之 Test Economics，希望能建構一軟體系統，考量各 IP 特性與測試機之規格與限制，對一系統晶片之測試成本效益能有一預估並做最佳化。

由上所述可知，各子計畫於本整合計畫各佔地位且環環相扣，互為幫補。計畫之完成將對國內 SOC 驗證及測試技術之提升有幫助。

三、結果與討論

(1) System-level verification interacting with architecture exploration:

In this sub project, our front-end verification environment and its associated tool have successfully overcome the challenges of IP-based architecture exploration mentioned at the beginning of this report. The reasons are:

1. The communication between hardware and software instances is highly feasible because both hardware and software instances are modeled at the same level of abstraction and the simulation environment views hardware and software instances as homogeneous models.
2. The performance estimation of the architecture is fast and accurate because our time-faithful modeling technology saves a large amount of simulation time, by not modeling the processing data and their transforms.
3. The selection of IP cores is efficient because the architectural attributes can be rapidly tuned to find suitable architecture specifications. Furthermore, **RIPÉE** can also determine suitable architectural attributes without using existing IP cores. This allows designers to use the attributes to define IP specifications.

(2) Functional verification techniques for IP-based SOC design:

In the sub project 2, we have built the framework of our verification system. It can take gate-level Verilog as input. We developed our algorithms and system based on two embedded processor IP designs: a simple pipelined Floating Point Unit (FPU) and a commercial product “embedded Sparc Processor”. After studying the design of the simple pipelined FPU design, we have developed an efficient verification algorithm and implemented into our verification system. We have verified some properties of the simple FPU design and found several bugs in the design. We also studied the embedded Sparc processor design and converted the RTL design in gate-level format for our verification. After converting it, we will apply the same verification method to verify the FPU in Sparc processor. Experimental results show the usefulness of our algorithms and system. Besides, we have written several papers based on this research work [1-3].

(3) Testing technology development for IP-based SOC design:

For the first year of the sub-project, there are six topics under investigation. For all the topics, significant progress has been obtained and some of results are being or have been written into papers for publication or for application for patents:

1. “Stuck-at and open/short” testing on IP interconnection wires and 2. Coupling (noise) fault testing between IP interconnection:

In IP-based SOC design environment, all IP's are assumed to be designed with IEEE1149.1 boundary scan and connected in P1500 format. For the above two topics, an innovative scheme has been invented which can detect both the above two classes, i.e., “stuck-at and open/short”, and “coupling” faults of interconnection lines of IP's. Through modifying boundary scan cells of each IP, we can construct oscillation rings on selecting interconnection lines of IP's. By observing oscillation of rings, we can detect

all the stuck-at and open/short faults of the connected interconnection lines. By observing if there are oscillation signals of the neighboring interconnection lines, we can detect the coupling faults between the oscillating interconnection lines and the neighboring interconnection lines. Furthermore, with some additional modification on the oscillation detection circuit to detect the period of the oscillation signal, the delay of the interconnection lines can be measured. This offers an additional way to detect delay faults of interconnection lines.

3. A BIST scheme based on oscillation ring test for combinational digital IP's:

For this topic, instead of using the original idea of forming oscillation ring to detect stuck-at and delay faults for combinational IP's, we invent a "Socillator" scheme to detect the above faults. The scheme is neat and powerful. The idea is to use an oscillation source, from which the name "Socillator" comes from, to be fed into the path-under-test (PUT) of the combinational IP with the pattern for other inputs of the IP shifted from the boundary scan chain. A detection circuit is designed to catch the transition of signal propagating through the PUT. By varying the period of oscillation source, the delay of the PUT can be tested. This offers a way to detect the delay fault of a combinational IP without using an external ATE. The scheme has been written into a paper and accepted for presentation in VTS2001 [4], and been filed for patenting.

4. Oscillation ring test for sequential IP's:

Sequential IP's intrinsically have a potential to oscillate when their state variable outputs are connected directly to their corresponding inputs. Through oscillation of the connected oscillation rings, the stuck-at faults of the associated lines with the oscillation rings can be detected since existence of those faults will stop the oscillation, and the delay of connected paths

can be tested if the period of the oscillation is measured. An algorithm to select the feedback paths to be connected has been developed to make the sequential IP oscillate under fault-free condition. Also, the flip-flops of the circuit are modified to have four different modes in order to insert additional inversion in the feedback path to create oscillation. In addition, a test generator to generate hazard-free delay test pattern for the circuit-under-test is developed to facilitate this test scheme and a fault simulator is under development to evaluate the fault coverage of the generated patterns. Currently, benchmark circuits are test-run to verify the algorithm and the developed software packages. It is expected that the scheme offers an approach which is completely different from the current sequential circuit testing but powerful without using an ATE.

5. Delay test methodology for mixed-signal IP testing:

For this topic, we have proposed a new fault model and, based on the model, a test strategy for testing linear analog circuits. The proposed fault model is called OPA fault model, i.e., the fault effects of a linear circuit are lumped as the offset(O), phase(P), or amplitude(A), in addition to the delay time, of the output response of the circuit under the periodic input. Instead of measuring the whole waveform of the output response, we measure the OPA of the output signal as signatures of the CUT under the applied input periodic signal. This saves much testing time for analog circuits. A theoretical foundation for the scheme has been developed and several benchmark circuit examples are used to demonstrate the scheme. The results are compared with those of other test methods.

6. IDDQ testing to deep submicron VLSI considering process and device parameter variations:

For this topic, the IDDQ current of the deep sub-micron VLSI in Year 2011 is estimated with a statistical approach

considering process variations and device parameter deviations. The estimation is done with the reference to 1999 edition of International Technology Roadmap for Semiconductors. Also, during estimation, 2000 different input vectors are applied and simulated to find the statistical distribution of the IDDQ. The estimated results show that the standard deviation of the IDDQ current is proportional to the square root of the circuit size and the IDDQ currents of the defect-free and defective devices, which are of the gate count up to 10^7 ; and the defective IDDQ is still differentiable from the fault-free case under the condition of random process variations and input vectors. In addition, we have invented two new IDDQ testing schemes, which instead detect the magnitude of IDDQ of a single circuit, detect the difference of IDDQ's of two different circuits. This makes the IDDQ testing more effective in detecting faults.

The results of this study has been written into a paper and presented in ATS2000 [5]

(4) SOC silicon diagnostics and yield improvement:

茲將本年計畫進行之八項工作，並已達成規劃書所列的目標部份，分述於下：

1.設計與製程能力用於良率最佳化之分析：

本工作起因於探討製程能力相對於不同的設計規格的影響。其中使用到多變量分析的方法並將實例推衍至多變數及其相關性，從現有的數據顯示規格參數其相關性少許的變化可引起功能良率極大(可達 20~40%)的改變。

本工作已完成(二維變數)參數相關性對應於不同設計規格之功能良率評估，由此功能評估良率亦可做為設計最佳化的指標。在本工作中亦將繼續探討規格轉換、規格分割以及維數降低等問題，以利於從晶片、模組、電路、元件以至製程階層的良率評估。

2.測試機之性能分析：

本工作起因於探討測試機準確度無法

應付快速晶片測試其對測試良率與品質的影響。其中測試機的性能參數將以如整體測試準確度、邊緣位移準確度、解析度和精確度來構述，並著重在探討更清晰的量測環境和完整測試時序。因此結合完整測試時序的總體良率與品質得以評估。

本工作已完成資料論文搜集，正研讀整理中。本工作亦將進行準確度差的測試機是否可提昇其準確量度能力的探討。

3.完整測試時序之評量：

本工作起因於探討晶片測試時並非只一次的評量，而是一連串的。其中吾人要探討一連串的評量其間的相依性，以及其對測試良率與品質的影響。

本工作已完成一次評量的品質良率圖，使用者可依其需求得到某一製程能力、設計規格、測試能力、測試規格相對的良率與品質；反之亦然。現正規劃單規格與多規格的複次評量。

再者根據製程、測試能力參數以及設計規格，吾人欲嘗試使用一延伸測試電路來做為數位電路製造良率的評估。由此評估良率可用來充作製程參數偏易的診斷指標。

4.激突(Jitter)在高速數位電路通訊之影響分析：

本工作起因於時鐘激途的穩定度影響高速數位電路通訊的品質。其中吾人要加入時鐘激途與位偏(skew)於延伸測試電路中探討性能模型。使用 MatLab 完成激途產生器並利用其於電路行為模擬。

本工作已完成針對 IEEE 1394 (FireWire)架構的傳輸品質分析，驗證資料觸發編碼(Data-Strobe Encoding)傳輸方式的確是優於資料時脈(Data-Clock)傳輸方式，並探討內部激途源分配對於傳輸品質的影響。

5.一具從屬關係多變量常態分佈之強化隨機數產生器：

本工作起因於使用蒙地卡羅方法於良率評估時對從屬關係多變量常態分佈的需求。由於共變數矩陣應是正值限定(Positive

Definite), 產生一高維度和好性質的共變數矩陣是相當不易的。其中吾人欲利用懷特寧與倒懷特寧方法將一獨立矩陣轉換成所需之具從屬關係矩陣, 以利良率評估。

本工作已完成, 可產生數萬個具從屬關係多變量常態分佈的隨機變數。

6. 類比數位/數位類比轉換器之規格評估:

本工作起因於類比數位/數位類比轉換器會大量使用於系統單晶片中, 故先從其規格評估起, 進而做良率評估。其中吾人根據類比數位/數位類比轉換器建構階層式功能模型, 依此探討製程偏移對功能良率的影響。

本工作已初步完成, 吾人分析從元件參數, (如 V_{ref+} , V_{ref-} , R_1 , R_2 ...), 對應到輸出參數, (如 V_1 , V_2 , V_3 , V_4 ...), 再對應到規格參數, (如 Offset, Gain Error, INL, DNL...) 的靈敏度, 進而做容忍分析 (Tolerance Analysis)。

7. Sigma-Delta 轉換器之規格評估:

本工作起因於 Sigma-Delta 轉換器可使用於系統單晶片自我測試中, 故先從其規格評估起, 進而做良率評估。其中吾人根據 Sigma-Delta 轉換器建構階層式功能模型, 依此探討製程偏移對功能良率的影響。

本工作已完成資料論文搜集, 正研讀整理中。

8. 強化晶圓參數粹取器:

本工作起因於深次微米技術之參數不匹配性(mismatch)加大, 使得電路設計與良率評估變難。其中吾人欲分析批對批、晶圓對晶圓、晶片間和晶片內之參數不匹配性。架構一分佈式模型參數, 依此亦可加入延伸測試電路中, 有利於來做為各種電路行為的評估。

本工作已完成資料論文搜集, 正研讀整理中。

四、計畫成果自評

子計畫一：本計畫第一年已建立基礎成本與效能模型, 可有助於組織探索階段

完成驗證工作。本計畫之研究成果已發表下列兩篇國際會議論文與一篇國內會議論文[1-3]。另外, 部分研究成果將發表於 Canadian Journal of Electrical and Computer Engineering 第四季期刊。

經由本計畫之執行已培養六名碩士畢業生。該六名碩士畢業生目前服務於系統晶片相關之高科技企業。

子計畫二：。

子計畫三：本計畫第一年已建立智財單元本身與相互間連線的測試機制, 有助於後續計劃之執行。吾人已完成原提計劃之 83%, 並已發表於國內外之期刊[4,5]。

子計畫四：本計畫研究內容與原計畫目標相符, 尤其是在類良率模型的建立, 以此模型所做的良率評估, 可使吾人分段模擬, 其結果幾乎與不分段一致; 另外對於不同規格參數轉換的探討, 不僅可用於設計時做最佳化之指引(尤其是高靈敏度電路如: 高速數位電路、類比電路、高頻電路), 亦可用於測試圖樣產生時最佳測試參數選取以及測試圖樣減少的指引, 亦可用於晶片測試時做為晶片診斷的指引。是以本計畫在這一年度的工作中, 獲得豐碩的成果, 亦在許多項目上值得繼續延伸。

五、參考文獻

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