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行政院國家科學委員會補助專題研究計畫 ☒ 成果報告
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高階伺服器電源系統數位控制架構之研究

A Research on Digital Control Architecture for Advanced Server Power Supply Systems

計畫類別：☒ 個別型計畫 ☐ 整合型計畫

計畫編號：NSC 98-2221-E-009-181

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計畫主持人：鄒應嶼 教授

共同主持人：

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執行單位：交通大學電機與控制工程系

中 華 民 國 九 十 九 年 九 月 三 日

A Research on Digital Control Architecture for Advanced Server Power Supply Systems

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主持人：鄒應嶼 博士 國立交通大學電機工程系 教授

一、中文摘要

本研究提出一個混合信號的邊界模式功率因數修正交-直流轉換器，其中包含類比電流迴路以及數位電壓迴路。本研究同時提出一種新型的負載適應增益調適以及帶拒濾波器於數位電壓方法，使系統輸出電壓在不同穩態負載情況下可達到相同的動態響應，並提升迴路的頻寬但仍可使輸入電流具備低總諧波失真以及高功率因數。在類比電流迴路中，類比電流比較器磁滯比較區間對於輸入電流總諧波失真的影響進行分析，並選取適當的值。在數位電壓迴路中，類比數位轉換器量化效應會使電流命令波形失真，因此適當的取樣率以及量化元件的位元長度將被決定。本論文使用電路模擬軟體 PSIM 驗證所提出控制架構，並與實驗結果相互驗證所提出之控制架構的可行性、有效性。

關鍵詞：功率因數修正、相移脈寬調變、數位控制、互連效應、整合控制

Abstract

This research proposes a mixed-signal solution for the control of the power factor correction (PFC) front-end power supplies in applications to distributed power supply systems (DSP). This research develops a mixed-signal implementation technique for critical mode PFC AC-DC converter with load adaptive gain scheduling. The peak current mode control is applied and analyzed by using the analog circuit. This paper analyzes effect of the hysteresis band effect of the analog current comparator in current loop. In digital voltage loop, the proper quantization resolution of ADC is determined. The digital voltage controller uses a digital notch filter to achieve fast dynamic response and a low total-harmonic-distortion (THD) with

high power factor (PF). A load adaptive gain scheduling applies for maintaining same dynamic response of the output voltage at different load conditions change. The proposed mixed-signal PFC control scheme has been verified by using computer simulation with experimental results to validate feasibility.

Keywords: distributed power supply, power factor correction, mixed-signal, digital control, adaptive gain scheduling.

二、緣由與目的

由於科技發展迅速，數位化與網路化是現代家庭生活的基本需求，基本家電自動化與資訊設備都需要電源供應系統，提供高品質的電源與降低電源損耗是未來電源技術發展的基本前提。

應用於通信設備、伺服器及資料中心之電源供應系統具備高效率的能量傳送、高供電品質、低雜訊干擾、高可靠度，以及具有良好的線擾動及負載擾動穩健性。為了應付這些嚴苛的需求，通訊設備及伺服器電源系統已朝向分散式電源系統(DPS)的方向發展，圖 1 所示為分散式電源供應架構[1]-[3]。

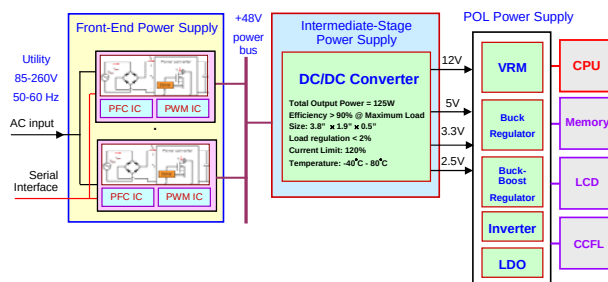


圖1 分散式電源架構

數位式伺服器電源控制系統整體方塊圖如圖 2 所示，包含前級功因修正 AC-DC 轉換

器與後級相移全橋 DC-DC 轉換器。功因修正 AC-DC 轉換器控制架構包含電流迴路，修飾輸入線電流波形，提高輸入功率因數，電壓本計劃擬發展整合功率因數修正 AC-DC 與相移脈寬調變之數位控制架構應用於高階伺服器電源之數位控制。

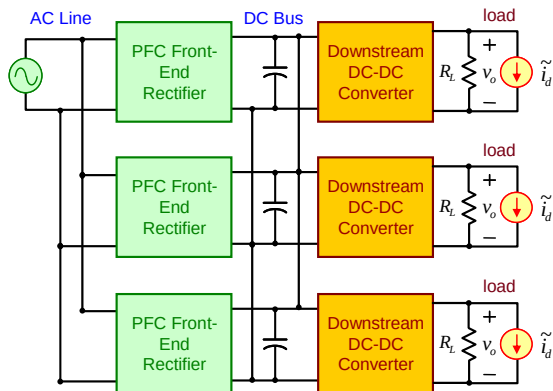


圖2 可並聯之分散式電源系統架構

伺服器電源通常採用分散式供電架構，前級為功率因數修正交流-直流轉換器，修飾輸入線電流波形以提高輸入功率因數，並轉換交流電壓至直流電壓且升壓至 400V，後級一般採用相隔離型相移脈寬調變全橋直流-直流轉換器，將 400V 電壓隔離並降壓至 48V 或 12V 的中間匯流排，透過控制加快輸出響應及提高效率。一般對於控制器設計都僅針對各級轉換器設計，串接兩級轉換器後再討論相互之間的影響[4]。

三、研究方法與成果

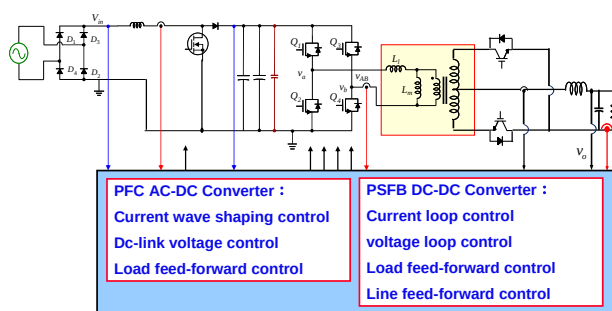


圖3 伺服器電源數位控制的系統方塊圖

圖 3 所示是一個典型的伺服器電源數位控制的系統方塊圖。主動式 PFC 轉換器必須藉由高開關頻率控制輸入的電流波形使其與線電壓同相，達到功率因數為 1.0 的目的，但此高頻切換也同時產生了額外的高頻電磁干擾，為了降低其傳導性電磁干擾，在其前端

必須加入適當設計的 EMI 濾波器。此濾波器與 PFC 轉換器所形成的迴路在某些工作條件或干擾信號可能會造成系統的不穩定。因此，濾波器與 PFC 的控制迴路設計均必須一起考量，確保電源的功率因數、電磁干擾與穩定性[5]-[8]。

目前純類比實現的功率因數控制晶片雖然可以達到輸入電流低諧波失真，但類比電路較易受到溫度的影響並且較難實現複雜的控制架構；而數位電路實現具有可程式化、長時間工作的穩定性以及較少的外加元件特性，可是數位電路受限於類比數位轉換器(analog-to-digital converter, ADC)和數位類比轉換器(digital-to-analog converter, DAC)取樣頻率以及解析度的影響，其準確度較低。

本研究針對如何整合類比電路與數位電路的優點進行控制架構設計。邊界導通模式的電流迴路為峰值電流控制，由於邊界導通模式開關為變頻操作並且在零電流處有高頻的開關切換，若數位電路實現則需極高頻的時脈因而造成大量的能量損耗，因此電流迴路以類比電路實現。電壓迴路頻寬通常不高，可以用低頻的時脈實現，並且為便於負載適應增益調變機制的實現，因此電壓迴路採數位電路實現。

迴路提供輸出直流鏈電壓穩壓，負載前向控制提高輸出響應速度而不致影響輸入線電流波形失真。而相移全橋 DC-DC 轉換器控制架構包含電流迴路，使電流具高頻寬，並可將系統特性由共軛根解耦為兩個實數根，可簡化電壓控制器設計，電壓迴路控制輸出電壓穩壓，負載前向控制提高輸出響應速度，輸入電壓前授控制可降低兩倍線頻漣波對輸出影響。

本研究提出一個混合信號控制的邊界模式功率因數修正交直流轉換器[9]-[12]，圖 4 為系統架構方塊圖，其中電流迴路以類比方式實現，電壓迴路則以數位電路實現。電壓迴路控制器中，電壓補償器為 PI 控制器，以消除輸出電壓穩態誤差；數位帶拒濾波器(notch filter)用以消除輸出電壓兩倍頻對於控制迴路的影響；由於在不同穩態狀況下，系統動態響應隨之變動，同樣大小的負載變動量，會有不同的暫態響應，因此加入負載適應增益調適使得不同負載狀況下同樣大小的負載變動量能有不同的暫態響應。

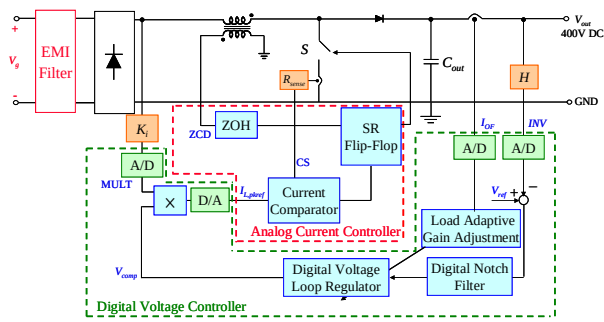


圖4 具負載增益調適混合信號控制之邊界模式功率因數修正交-直流轉換器系統方塊圖

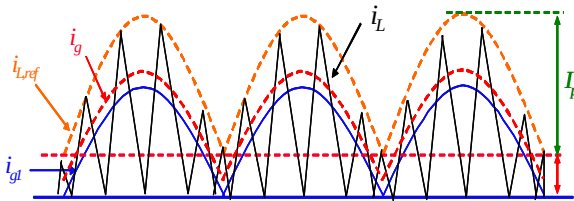


圖5 電感電流、線電流與線電流基頻成分的關係

類比電流比較器主要用以比較開關電流回授信號與電感電流命令封包，當開關電流回授信號頂到封包命令時，則關閉開關。在類比電流比較器設計上，為了降低雜訊的影響通常會加入一個磁滯比較區間，不過這個磁滯比較區間卻會帶給電感電流命令一個直流值的提升，進而使得輸入線電流在零交越處失真，因此選擇適當的磁滯比較區間使得此磁滯比較區間，使線電流滿足諧波規範。

電流比較器磁滯比較區間大小、線電流波形以及線電流基頻成分波形的關係圖如圖 2 所示；其中磁滯比較區間在電感電流封包中所造成的直流成分為 ΔH_1 ，線電流波形為 i_g ，而線電流基頻成分為 i_{g1} 。

根據分析可以推得磁滯比較區間與線電流的關係如圖 6 所示，而輸入線電流的大小通常可由設計者進行決定，因此可以決定適當的磁滯比較區間。在本論文中設定於滿載情況下線電流至少要低於 5%，則由圖 3 可以得知如要滿足此需求，磁滯比較區間至少需低於 65 毫伏，本文選取 50 毫伏。

在 PFC 數位電壓迴路的實現設計，整流後線電壓回授主要用以產生電感電流命令信號，其直接影響到電流命令的失真量，因此類比數位轉換器與數位類比轉換器的取樣頻率與量化效應需加以考慮。

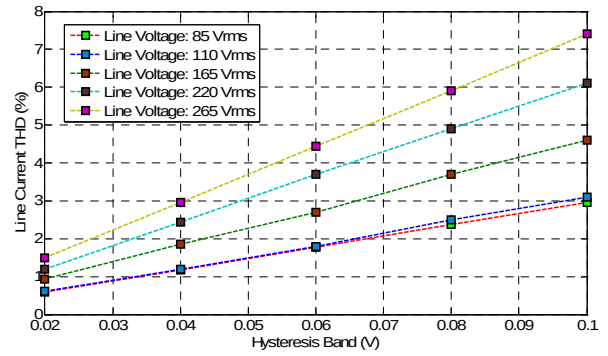


圖6 電感電流、線電流與線電流基頻成分的關係

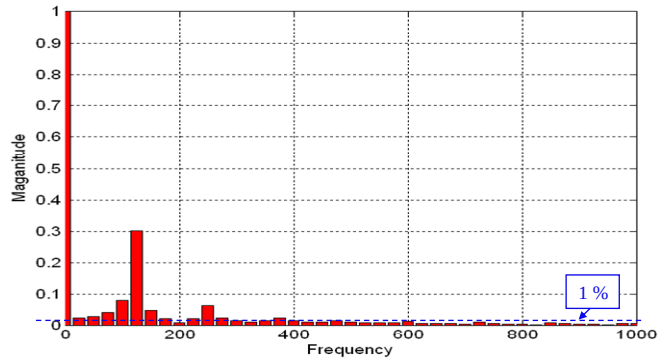


圖7 半弦波電流之頻譜

在取樣頻率的設定上，由信號處理中的取樣定理可知，當預取樣信號的頻譜如範圍在 ω_n 以內，而此時取樣頻率 ω_s 如小於兩倍的 ω_n 值，此時取樣後之信號會失真。在取樣頻率上欲使取樣後的整流弦波電流無明顯的失真，因此先對整流後的弦波信號進行頻譜分析，並假設頻譜中振幅小於 1% 的高階量可以忽略，由圖 7 可以發現當頻率到 1 kHz 時，頻譜的振幅大約小於 1%，可知取樣頻率至少需大於 2 kHz 才能使得取樣後的整流弦波波型較不失真，本研究選取 5 kHz 的取樣頻率。

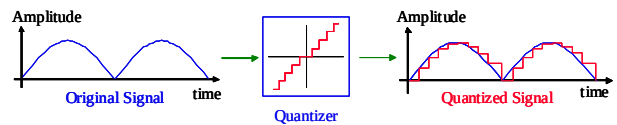


圖8 量化對於整流後弦波的影響

量化誤差對於一個整流後弦波波型的影響如圖 8 所示，當一個整流後弦波經過量化後，會呈現階梯狀的失真現象。而此量化效應可以等效為一個量化雜訊加入於控制系統迴路中。為了決定解析度所造成的量化雜訊影響，而有關量化誤差的模型，主要有兩種形式，一種為鋸齒波近似另一為方波近似，而其最壞的狀況為方波近似法，因此對方波

進行傅立葉轉換，可計算出此方波量化雜訊模型的最大誤差量。

根據 EN61000-3-2 中 Class C 的規範，可得知其對於線電流各諧波成分方均根值的限制隨負載不同而變化，必須小於 3% 的線電流方均根值。最壞的狀況發生於，線電壓有最小方均根時；如果此時 K_i 為 0.0052，則解晰度必須小於 0.025，因此在整流線電壓回授的類比數位轉換器，必須至少是 10 位元。

一般功率因數修正交-直流轉換器的電壓迴路頻寬通常不高，是為了消除輸出電壓兩倍頻的漣波對於控制迴路的影響；本文為了提升電壓迴路的頻寬並且仍能維持線電流為低諧波失真與高功率修正目的，因此在控制迴路中加入數位帶拒濾波器以有效的濾除輸出電壓兩倍頻漣波的影響，其系統方塊圖如圖 9 所示。當此帶拒濾波器的中心頻率(center frequency, ω_0)等於 λ 時，則該點頻率的信號將被完全濾除，其中分母的一階係數代表當其振幅掉至 3 dB 點的頻寬大小。藉由轉移函式欲求其中心頻率時可令振幅為零，而 3 dB 的頻寬則令轉移函式的振幅掉至其直流值以下 3 dB 的點，因此可設計出針對特定頻率所需衰減程度的帶拒濾波器。

加入帶拒濾波器使得不僅改善頻寬且能維持線電流低諧波失真與高功率因數的特性。由於在不同穩態負載狀況下，系統的動態響應也會隨之變動，因此在不同穩態負載下變動相同大小的負載量其回復時間也不同；為了使系統於不同穩態負載下變動相同大小的負載量皆能有同樣的回復時間，本文提出負載適應增益調變機制。

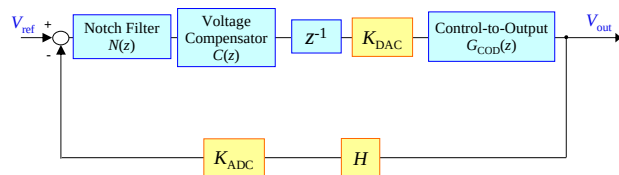


圖9 加入帶拒濾波器之系統方塊圖

負載適應增益調變機制主要利用查表法並搭配內插法，並且增加輸出電流回授，當負載變化時，控制器的參數也隨之改變。此可隨負載波動而調整之適應性數位 PI 控制器基本上是一個控制參數根據不同操作點所設計的控制器，主要在於根據不同負載調整期相位補償頻率，此控制器之參數如表 1 所示。

表1 查找控制參數表

Load (%)	10	30	50	70	90
i_{out} (A)	0.025	0.075	0.125	0.175	0.225
α	1	1.036	1.072	1.108	1.114
β	1	1.0005	1.001	1.0015	1.002

圖 10 與圖 11 分別代表輸出電壓暫態響應在未加入負載適應增益調適與加入負載適應增益調適機制；在圖 11 中，還未加入負載適應增益調變，其由 10 W 變動於 50 W 時回復時間為 43 ms，而由 60 W 升至 100 W 時回復時間為 30 ms；當加入負載適應增益調適機制後，不管是 10 W 變動於 50 W 或是 60 W 變動至 100 W 情況下，系統動態響應回復時間皆為 30 ms，因此證實加入負載適應增益調適機制後，確實能有效的改善系統於不同負載下之動態響應。

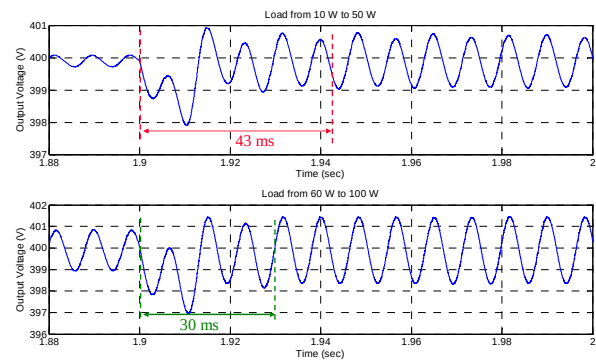


圖10 加入負載適應增益調適輸出電壓暫態響應，負載分別由10瓦到50瓦以及60瓦到100瓦

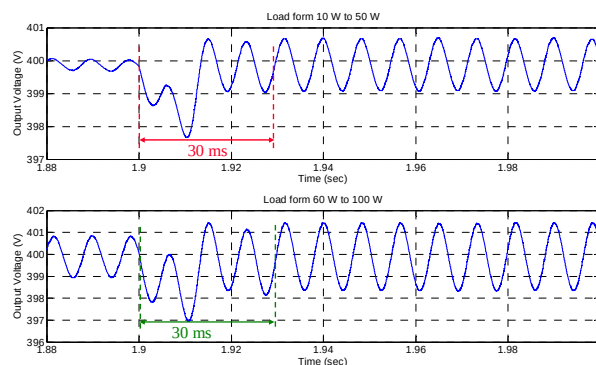


圖11 加入負載適應增益調適輸出電壓暫態響應，負載分別由10瓦到50瓦以及60瓦到100瓦

四、結論與討論

本研究提出一個混合信號的邊界模式功率因數修正交-直流轉換器，其中包含類比電流迴路以及數位電壓迴路。電流比較器磁滯比較區間的值定為 50 mV；數位電壓迴路控制中，類比數位轉換器選用 8 位元，取樣頻率為 5 kHz，而數位類比轉換器則選用 10 位元；並加入數位帶拒濾波器以提升動態響應，並維持線電流低諧波失真與高功率因數；而負載適應增益調適機制，用於改善不同穩態情況下的，等量負載變化，使其動態響應相同，經由模擬與實驗驗證本研究提出方法之可行性。

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可供推廣之研發成果資料表

■ 可申請專利

■ 可技術移轉

日期：99 年 9 月 23 日

國科會補助計畫	計畫名稱：高階伺服器電源系統數位控制架構之研究 計畫主持人：鄒應嶼 計畫編號：NSC 98-2221-E-009-181 學門領域：電力
技術/創作名稱	混合信號功率因數修正控制技術
發明人/創作人	鄒應嶼
技術說明	中文： 本技術『混合信號 PFC 控制技術』針對單相之交直流電源轉換系統發展結合數位類比混合訊號電路實現的 PFC IC 核心技術，可應用於升壓式交直流轉換電路功因校正控制晶片之設計，採用混合信號控制架構，主要包含數位 PWM 產生電路、類比電流控制、與數位相位補償控制電路。
	英文： The developed mixed-signal power factor correction technique can be applied to single-phase ac-dc converter with unit power factor correction. The developed technique can be used for boost ac-dc converter for power factor correction and voltage regulation. The developed technique can be used to realize cost effective high performance PFC control IC.
可利用之產業 及 可開發之產品	開關式電源供應器、電源設備之數位控制 不斷電系統、功率因數改善設備 電源管理 IC、照明 IC、數位電源 IC、PFC IC、數位 PWM IC
技術特點	■ 混合信號 PFC 控制技術 ■ 數位式脈寬調變產生電路、類比電流控制 ■ 可應用於非隔離式升壓型交直流 PFC 轉換電路 ■ 可應用於 PFC IC 之實現 ■ 可應用於電源管理 IC
推廣及運用的價值	混合信號 PFC 控制技術可廣泛應用於各類需要連接市電之電源設備，本技術提供混合信號 PFC 控制晶片設計的系統架構設計與實現方法，並以 DSP 與類比電路完成系統整合驗證，可進一步推廣於各類與市電連結電源系統之應用，或提供 PFC IC 設計之 IP。

- ※ 1.每項研發成果請填寫一式二份，一份隨成果報告送繳本會，一份送 貴單位研發成果推廣單位（如技術移轉中心）。
- ※ 2.本項研發成果若尚未申請專利，請勿揭露可申請專利之主要內容。
- ※ 3.本表若不敷使用，請自行影印使用。

出席國際學術會議心得報告

計畫編號	98-2221-E-009-181
計畫名稱	高階伺服器電源系統數位控制架構之研究
出國人員姓名 服務機關及職稱	鄒應嶼 教授／國立交通大學電機工程學系
會議時間地點	98 年 9 月 19 日至 9 月 24 日／美國加州舊金山聖荷西市(San Jose, CA)
會議名稱	2009 IEEE Energy Conversion Congress and Expo 2009 年國際能源轉換論暨展覽研討會
發表論文題目	Chia-Hao Wu and Ying-Yu Tzou, "Digital control strategy for efficiency optimization of a BLDC motor driver with VOPFC," <i>IEEE ECCE Conf. Rec.</i> , San Jose, CA USA, Sept. 21-25, 2009.

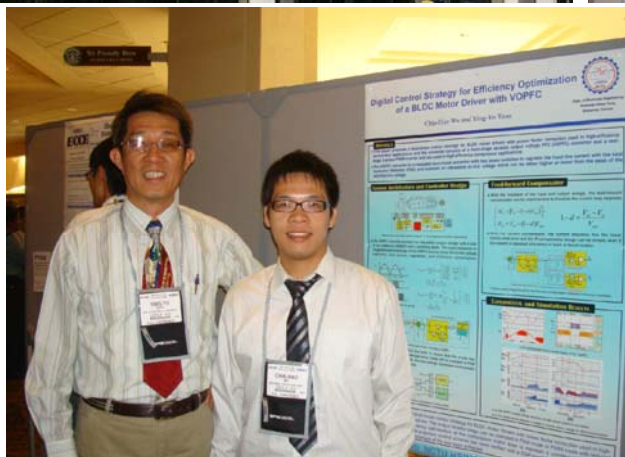
一、參加會議經過

本人 2009 年 9 月 19 日前往美國舊金山參加 ECCE2009 學術研討會，此研討會是由國際電機電子工程學會(IEEE)之電力電子學會(PES)與工業應用學會(IAS)所主辦的首屆 IEEE Energy Conversion Congress and Expo，此研討會係結合了 PESC Conference 及 IAS Annual Meeting 兩大年度重要學術研討會，主要針對『能源』為主題，其領域跨及的技術層面涵蓋了電力電子、電池儲能、綠色能源、電源 IC 等相關領域。此次研討會於今年 9 月 19 日至 24 日在美國加州聖荷西市(San Jose, CA) 的 DoubleTree Hotel 舉行，有將近 900 位來自 40 幾個國家的與會者，此次邀稿大會收到超過 1200 篇的投稿論文，挑選了近 600 篇論文。而其兩天的展覽也吸引了近 30 家相關領域的廠商參與展出。

本研討會是電力電子領域最重要的國際學術研討會之一，較著重於學術理論發展，是新理論與新方法論文發表的重要學術研討會。此次議程包括：直流-直流轉換器、直流-交流轉換器、馬達驅動器、數位控制技術、電池儲能、綠色能源、電源 IC、功率模組整合封裝技術、高功率直流轉換器、電磁干擾等等。此次與會除了發表論文外，亦與國際友人聯絡友誼、交換意見，瞭解這些領域之研究動向與未來發展之趨勢。

二、與會心得

本次研討會著重於綠色能源的發展，特別是太陽光發電、馬達節能技術受到重視，也有專屬的議程討論。整合類比電路設計與電力電子的應用發展，近年來逐漸受到重視，小型電源控制與轉換 IC，如充電 IC、電源管理 IC、小型馬達驅動 IC 等等，都具有廣大的市場發展潛力。交通大學電力電子實驗室本次發表之論文研究著重於數位式電源轉換與馬達控制 IC 技術之研究與發展，政府目前積極推動綠色能源計畫，鼓勵以電力電子與綠色能源為導向的系統整合，國內電力電子領域設計人才濟濟，或可結合綠色能源、太陽光電、風力發電、電源設計、馬達驅動、IC 設計人才，從資訊家電的綠色能源技術領域著手系統整合的研究。



大會會場、全體大會報告、展示會場、大會晚宴、攜回資料

Digital Control Strategy for Efficiency Optimization of a BLDC Motor Driver with VOPFC

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Abstract—This paper proposes a dual-mode control strategy for BLDC motor drivers with power factor correction used in high-efficiency compressor applications. The motor driver consists of a front-stage variable output voltage PFC (VOPFC) converter and a rear-stage 3-phase PWM inverter. The VOPFC converter is a cascaded buck-boost converter with two power switches to regulate the input line current with low total harmonic distortion (THD) and at the same time to maintain an adjustable dc-link voltage which can be either higher or lower than the peak of the rectified line voltage. The output inverter stage can be operated in pulse amplitude modulation (PAM) mode or PWM mode with reduced switching frequency for efficiency optimization of the compressor motor driver to maintain a constant V/Hz ratio with specified current ripples. The proposed control scheme has been verified with a DSP-controlled VOPFC PWM/PAM motor driver and an efficiency improvement of 3% has been achieved.

Index Terms—variable output power factor correction (VOPFC), brushless dc motor, compressor driver, dual-mode control, efficiency optimization.

I. INTRODUCTION

BLDC motors have been widely used in various applications, and they have a better efficiency and produce more power for the same size compared to induction motors. For the rotated speed of the motors, the bus voltage of the inverter needs high enough to overcome the back-EMF that is proportional to the speed. The traditional motor drivers are designed as fixed-voltage-control, so the switching frequency of pulse width modulation (PWM) is up to 16 kHz to rotate motors for lower current ripples. However the high switching frequency is always along with the large switching losses [1]. Besides, when the motor rotates in slow speed, the duty cycle of PWM module in inverter must be low consequently and the extreme duty cycle may have a greater distortion in the voltage control for the dead time control.

Moreover, it is well known that power supplies connected to AC without power factor correction will introduce high low-order harmonic currents and result in poor power quality. Such harmonic currents cause several problems including voltage distortion, heating, radiated and conducted noises and can reduce the capability of the line to provide energy. Recently the demands for high power factor and low harmonic distortion in the current drawn from the utility have been increasing [2]–[3]. As a result, in order to meet the

requirements of high power factor and high efficiency in modern motor driver, the control strategy for high power factor correction and efficiency optimization with the integration of VOPFC and inverter has been developed [4–6].

Boost converter is usually employed for the single-phase PFC applications, as shown in Fig. 1(a). But its fixed dc-link voltage will result in higher switching losses at light load under low speed operation of the compressor driver. In order to improve the compressor driver at low-speed operation region, a lower dc-link voltage with minimum switching frequency is preferred. The VOPFC converter is a buck converter cascaded with a boost converter shared with a common inductor, and the schematic of the VOPFC inverter driver is shown in Fig. 1(b).

The VOPFC converter provides an adjustable output voltage with a cost of one additional MOSFET and a switching diode. This paper proposes an integrated control strategy of the VOPFC inverter driver for dc-link voltage regulation, line current regulation, and efficiency optimization. The design and implementation of the VOPFC controller are presented and their benefits and limitations are analyzed.

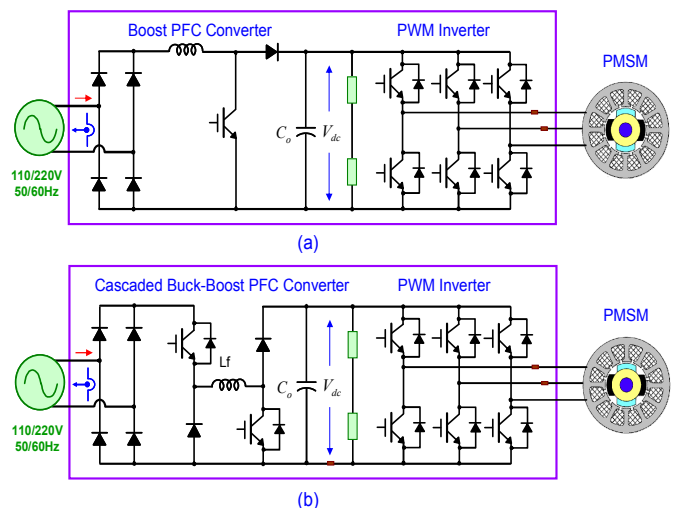


Fig. 1. Two PFC AC/DC converter topologies for compressor PMSM drivers (a) boost converter (b) cascade buck-boost converter.

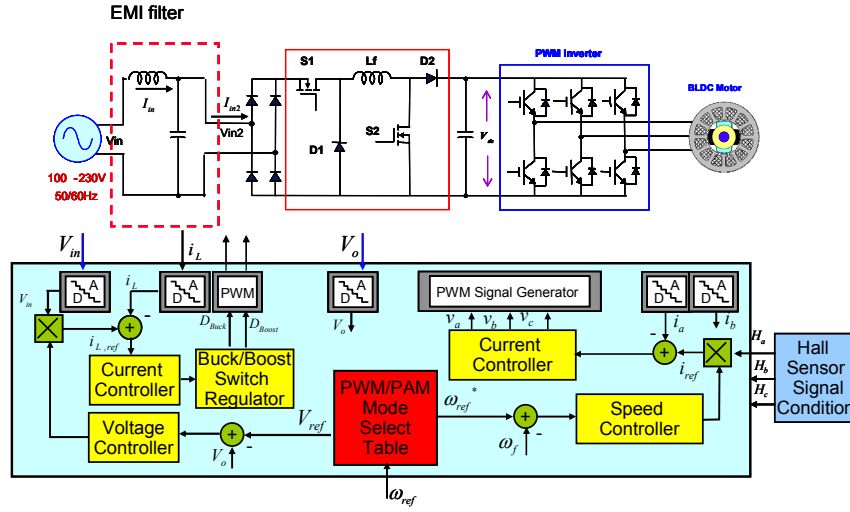


Fig. 2. Circuits and control system diagram in the integration of VOPFC and inverter.

II. SYSTEM ARCHITECTURE

This paper proposes the design of VOPFC converter applied to household compress drivers. We selected the circuit of cascaded buck-boost to realize the VOPFC, because the lower cost in the cascaded buck-boost topology lower than in the buck-boost one for reduced size inductor and capacitors can be used [7]. The circuit architecture and system control diagram are as shown in Fig. 2. We cascade the VOPFC converter and an inverter to form a two-stage BLDC motor driver.

As shown in Fig. 3, when input voltage is higher than output voltage, the VOPFC converter is operating in buck mode via buck-switch (S1) to generate the output voltage. On the contrary, when input voltage is lower than output voltage, the system is operating in boost mode via boost-switch (S2) to generate the output voltage.

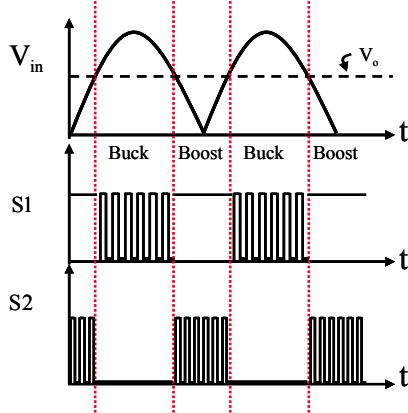


Fig. 3. Duty cycle and status of switch S1 and S2.

With the feedback of the motor's speed and phase current, BLDC motor can be controlled in steady speed and maintain

constant torque. When the compressors work at a relatively low speed, the back-EMF of motor is low. With the VOPFC converter, the bus voltage can be decreased, so the inverter avoids the high switching frequency consuming redundant switching loss to improve the efficiency of the compressor motor. Otherwise, in order to speed up the response of acceleration, the bus voltage increases to meet the back-EMF that is proportional to speed and the inverter is operated in PWM mode.

The inverter controller consists of an inner current loop controller and an outer speed loop controller. The current loop controller regulates motor phase currents with specified current ripples and generates PWM signals according to the Hall-sensor feedback. The speed controller generates a torque current command according to an estimated speed feedback from the measured Hall-sensor feedback. When the motor is running in constant speed mode, the inverter controller can be operated in PAM mode to minimize switching losses or PWM mode to minimize torque ripples with specified current profile.

III. VOPFC CONTROL STRATEGY AND CONTROLLER DESIGN

Fig. 4 is the control block diagram of the cascaded buck-boost converter. The system controller is designed to be multi-loop and it includes the current controller and voltage controller. In order to achieve PFC, the input voltage and the input current should be maintained in-phase. The system uses input voltage as the reference to control inductor current. In the cascade buck-boost circuit, its operation is changing adaptively between buck and boost mode. In order to speed up the response of current loop, a feed-forward compensation controller is employed. It linearizes the transfer function of the current loop in VOPFC converter and simplifies the design of current controller.

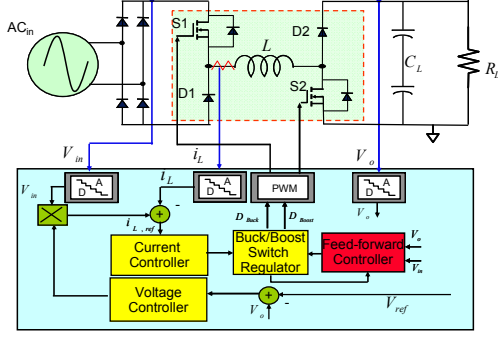


Fig. 4. The cascade buck-boost converter with control block diagram.

A. Small signal analysis and controller design

Due to the need of operating between buck mode and boost mode with the input voltage being a semi-sine wave, a non-static voltage source, the controller design must be considered in different operating points. The current control block diagram is two stages in the system. First stage is a PI controller and second stage is the feed-forward compensation controller.

Before the designing PI controller, the transfer functions of buck and boost modes should be obtained firstly by the state-space averaging method. In boost mode, the transfer function of the converter can be expressed as

$$T_{p,Boost}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = [1 \quad 0] \times \begin{bmatrix} s + \frac{1}{R_L C_L} & (1-D) \\ \Delta(s) & L\Delta(s) \\ (1-D) & s \\ C_L \Delta(s) & \Delta(s) \end{bmatrix} \times \begin{bmatrix} \frac{V_o}{L} \\ \frac{-I_L}{C} \end{bmatrix} \quad (1)$$

$$= \frac{V_o(1-D)}{L \times \Delta_1(s)} - \frac{sI_L}{C_L \times \Delta_1(s)}$$

By the same method, the transfer function for buck mode can be expressed as

$$T_{p,Buck}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = [1 \quad 0] \times \begin{bmatrix} s & \frac{1}{L} \\ -\frac{1}{C_L} & s + \frac{1}{R_L C_L} \end{bmatrix} \times \begin{bmatrix} \frac{V_{in}}{L} \\ 0 \end{bmatrix} \quad (2)$$

$$= \frac{1}{\Delta_2(s)} \frac{V_{in}}{C_L \times L}$$

where $\Delta_1(s)$ and $\Delta_2(s)$ are

$$\Delta_1(s) = s^2 + \frac{s}{R_L C_L} + \frac{(1-D)^2}{LC_L} \quad (3)$$

$$\Delta_2(s) = s^2 + \frac{s}{R_L C_L} + \frac{1}{LC_L} \quad (4)$$

The above equations show that the transfer functions of the buck and boost converters are both second-order systems.

The transfer function of boost has a zero but the one of buck doesn't. After calculating the transfer functions of boost and buck, the bandwidths of current control loop under different operating points are distinctly discussed. Analyzing the small signal models of buck and boost circuit under variable input voltage, the minimal bandwidth and worst response appeared at the border of buck and boost. The bode plots of the buck and boost are shown in Fig. 5. The SISO tool in the MATLAB was used to synthesize the compensation zero of PI controller for the current loop. The goal for design of current controller would increase the bandwidth of current loop to improve response speed.

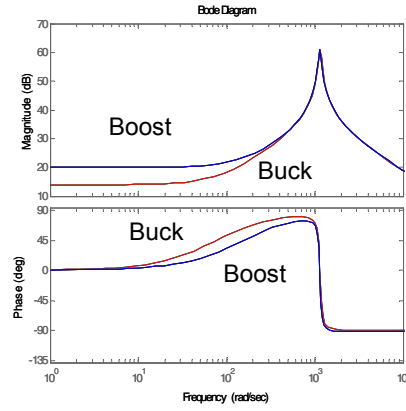


Fig. 5. The bode plots of the transfer functions of buck and boost when input voltage is 100V.

After designing the first stage current controller, the feed-forward compensation controllers in second stage were designed independently for buck mode and boost mode.

B. Feed-forward Compensation Controller

In order to let the system have the quicker speed of response, the paper proposes the design of the multi-loop controller for the buck-boost circuit as shown in Fig. 6. The minor loop is current control and the major loop is voltage control. In order to linearize and improve the current response, the feed-forward compensator controller is designed as shown in Fig. 7. With the current compensator, the current response has the lower steady state error and the PI compensator design can be simple, even if the system is operated alternately in buck or boost modes.

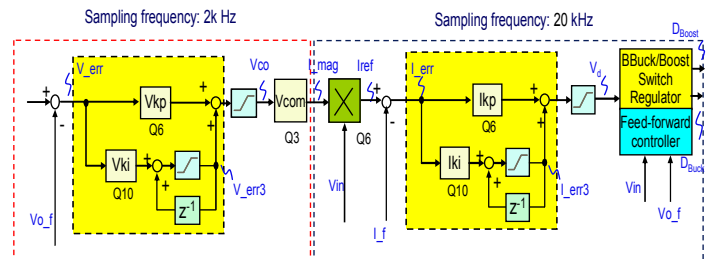


Fig. 6. Current controller and voltage controller in VOPFC.

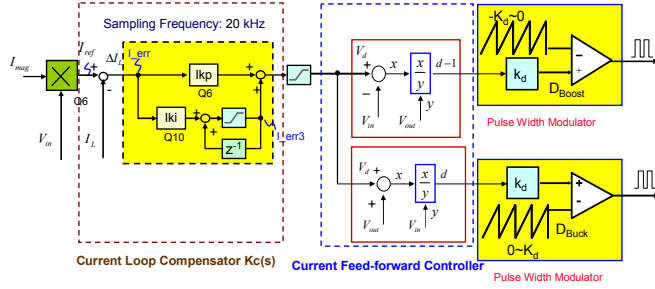


Fig. 7. System block diagrams of the feed-forward compensator controller and current controller.

After designing the first stage current controller, the second-stage was continuously designed separately for buck and the boost circuit characteristics.

When system is operated in boost mode, the current incremental ΔI_L in the input inductor during a PWM switching period T_s with duty ratio of d can be expressed as

$$\Delta I_L = [V_{in} - (1-d)V_{out}] \frac{T_s}{L}. \quad (5)$$

This is the desired voltage that we need to apply to the inductor, let's denote as V_d . It can be expressed as

$$V_d = V_{in} - (1-d)V_{out}, \quad (6)$$

where V_d is the output of the PI controller $K_C(s)$ and it is the command of the voltage that we want to apply to the inductor to result a increment current to reduce the current error as shown in Fig. 7.

$$\frac{V_{in} - V_d}{V_{out}} = 1 - d \quad (7)$$

The PI current compensation controller $K_C(s)$ can improve the steady state error.

The consideration in buck mode is similar with boost mode. V_d is the output of the PI current loop controller $K_C(s)$, which is the voltage we want to apply to the inductor to result a current increment of ΔI_L to reduce the current error.

$$\frac{V_d + V_{out}}{V_{in}} = d \quad (8)$$

With the employment of the feed-forward compensator for the current loop regulation, the current response can be improved significantly to achieve low current harmonic distortion.

C. Inductor current command compensation

When the system is operated in boost mode, buck-switch (S_1) is constantly conducted and input current is equal to inductor current. The ripple of inductor current can be reduced by selecting the proper inductance, hence decreasing the THD of the input current. However, during the buck mode, the current through S_1 is the input current, and it is

intermitted due to the switching of power switch. As a result, an EMI filter is required to decrease THD to improve PF.

As known from the above, if the duty cycle of switch S_1 is D_{Buck} , the input current can be calculated by

$$I_{in} = D_{Buck} \times I_L \quad (9)$$

where I_{in} is the input current and I_L is the inductor current. If the inductor current command maintains the waveform as sine-wave, the input current will be non-sine-wave. Consequently, a compensation of inductor command is required in buck mode.

Because the input voltage V_{in} is converted into a stable DC voltage from a rectified semi-sine-wave via converter, according to the characteristic of buck converter, during continuous current mode (CCM), operation status of the system are as the following.

$$V_{in} = V_d \sin(\omega t) \quad (10)$$

$$D_{Buck} = \frac{V_o}{V_{in}} \quad (11)$$

$$I_{in} = D_{Buck} \times I_L = \frac{V_o}{V_d \sin(\omega t)} \times I_L, \quad (12)$$

where V_o is input voltage and D_{Buck} is the duty of S_1 .

From (12), if inductor current I_L is proportional to input voltage, the input current will be the constant value and the waveform will be distorted. As a result, a current compensation is implemented to eliminate this problem. In according to (12), inductor current command I_{L_ref} in buck mode is corrected as the following:

$$I_{L_ref} = K_d \sin(\omega t) \times \frac{1}{D_{Buck}} \quad (13)$$

From (12) and (13), it can be suggested that input current becomes sine-wave after compensation, as shown in Fig. 8.

IV. INTEGRATION SYSTEM DESIGN

A. Inductor ripple current analysis

During operation of a motor, the current is proportional to output torque and back EMF is proportional to the rotation speed. As shown in Fig. 9, ripple current I_a is Δ_i , during this operation condition, I_a pass through switches S_1 and S_6 or S_2 and S_6 . Because the current flow through two switches simultaneously, the switching conduction loss is analyzed as follows:

$$\Delta_i = \left(\frac{V_{dc} - V_\epsilon}{L_s} \right) \times D \times T_s \quad (14)$$

$$I_{RMS} = I_{avg} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta_i}{I_{avg}} \right)^2} \quad (15)$$

$$P_{C_Loss} = I_{RMS}^2 \times R_{ds_on} \times 2 \propto I_{RMS}^2 \quad (16)$$

Above equation suggests that switch conduction loss is related to ripple current in identical switching component. Switch conduction loss can be controller if inductor ripple current is controlled.

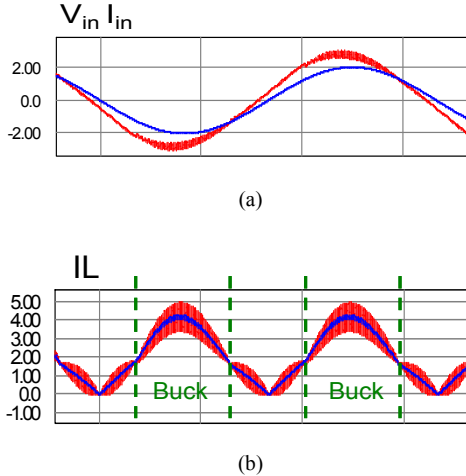


Fig. 8. (a) Input current and input voltage and (b) inductor current command and inductor current in VOPFC converter.

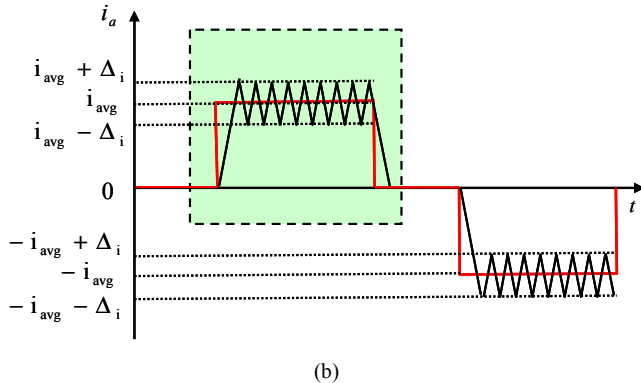
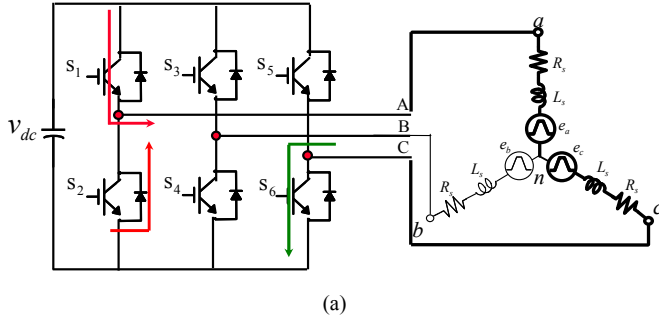


Fig. 9. (a) Schematic of the inverter and the BLDC motor. (b) Illustrated waveform of phase current under closed-loop PWM control.

Assuming speed and load torque of motor are constant, and back-EMF V_ϵ is proportional to motor speed. The motor controller is operated under different bus voltage V_{d1} and V_{d2} , the current ripples can be calculated from (14), and the relationship of Δ_{i1} and Δ_{i2} is expressed as

$$\frac{V_{dc1} - V_\epsilon}{L_s} \times \frac{V_\epsilon}{V_{dc1}} \times T_{s1} = \frac{V_{dc2} - V_\epsilon}{L_s} \times \frac{V_\epsilon}{V_{dc2}} \times T_{s2}. \quad (17)$$

$$\frac{T_{s1}}{T_{s2}} = \frac{V_{dc2} - V_\epsilon}{V_{dc1} - V_\epsilon} \times \frac{V_{dc1}}{V_{dc2}} = \frac{1 - \frac{V_\epsilon}{V_{dc2}}}{1 - \frac{V_\epsilon}{V_{dc1}}}, \quad (18)$$

where T_{s1} and T_{s2} are the periods of stitching.

According to the above equations, as motor drive is operated under a lower bus voltage, the switching frequency decreases accordingly to maintain the same level of inductor current ripple with the same conduction losses of power switches, and switching loss decreases significantly to improve the efficiency.

Fig. 9(a) and Fig. 10 show that high side switch and low side one switch alternately under a fixed switching frequency. During the transition of switching of power switches, the voltage waveforms and the current one overlap and result the switching losses in power switches [8]. The losses P_{s_Loss} after one complete cycle are calculated.

$$P_{on} + P_{off} = \frac{V_{dc} i_1}{2} \times t_{d_on} + \frac{V_{dc} i_2}{2} \times t_{d_off} \quad (19)$$

Assuming $t_{d_on} \approx t_{d_off} = t_d$

$$P_{s_Loss} = \frac{P_{s_on} + P_{s_off}}{T_s} = \frac{(i_1 + i_2)}{2} \times V_{dc} \times t_d \times f_s, \quad (20)$$

$$= i_{L,avg} \times V_{dc} \times t_d \times f_s \propto V_{dc} \times f_s$$

where i_1 and i_2 are the maximum and minimum of the inductor current, t_d is switching overlap, and f_s is the switching frequency.

From (18) and (20), the ratio of switching losses in different bus voltages can be expressed as

$$\frac{P_{s1}}{P_{s2}} = \frac{V_{dc1} \times f_{s1}}{V_{dc2} \times f_{s2}} = \left(\frac{V_{dc1}}{V_{dc2}} \right) \times \frac{T_{s2}}{T_{s1}}$$

$$= \left(\frac{V_{dc1}}{V_{dc2}} \right) \times \left(\frac{1 - \frac{V_\epsilon}{V_{dc1}}}{1 - \frac{V_\epsilon}{V_{dc2}}} \right) = \frac{V_{dc1} - V_\epsilon}{V_{dc2} - V_\epsilon}. \quad (21)$$

From (21), the relationship between the bus voltage V_{dc} and switching loss P_{s_loss} with the same back-EMF V_ϵ is shown in Fig. 11.

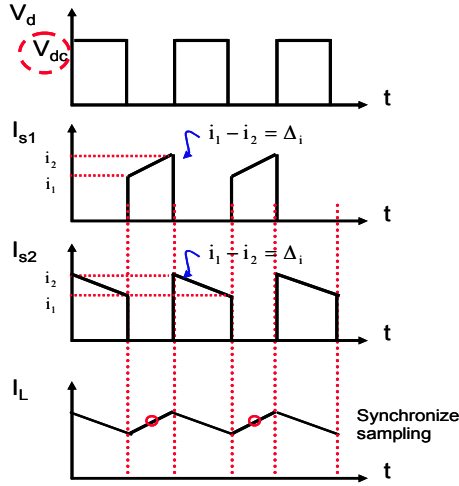


Fig. 10. V_d is the voltage across source and drain of the switch, I_{S1} and I_{S2} are switching current of switch $S1$ and $S2$, and I_L is the phase current of the motor.

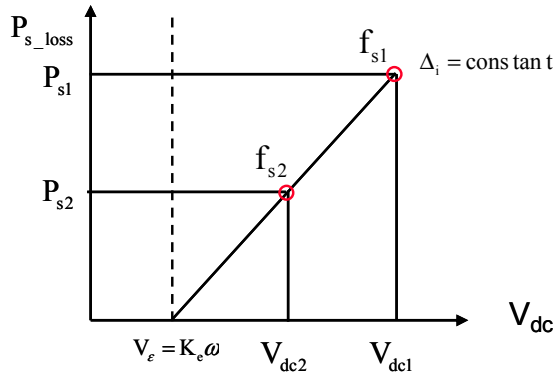


Fig. 11. The relationship between bus voltage V_{dc} and switching loss under the restriction that the current ripple Δ_i is the same.

Fig. 11 shows the results of the above equations, and we can understand that when the system is operated in steady speed, switch conduction loss is decreased via decreasing VOPFC output voltage or even instruct the system to work in PAM mode. On the contrary, the bus voltage is increased to improve current response when the system needs to accelerate. Required frequency modulation is realized by the usage of DSP 2407A micro-controller, which allows rapid variation of operation frequency. The hysteresis comparison look-up table of operation frequency for PWM modulation in different bus voltage is shown in Fig. 12.

B. Mode selection controller

The mode selection control block diagram is designed as shown in Fig. 13. If the speed error is less than the limit, it means that the motor has rotated in steady speed and the operation mode will be changed to PAM mode. In PAM operation mode, the bus voltage decreases continuously until the PWM module is full duty [9]. At this time, the output voltage of VOPFC converter is as low as the back-EMF of

motor and the switching frequency of the inverter is as low as the electric frequency of the motor. On the contrary, if the speed command varies, the speed error will be higher than the limit suddenly and the operation mode will be changed to PWM mode.

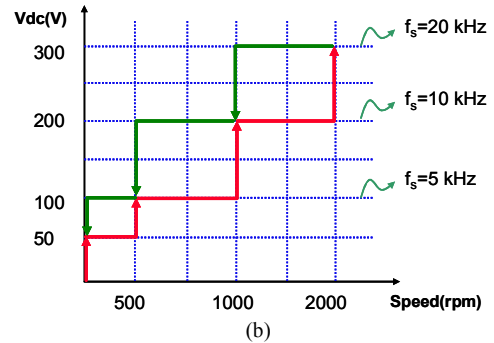
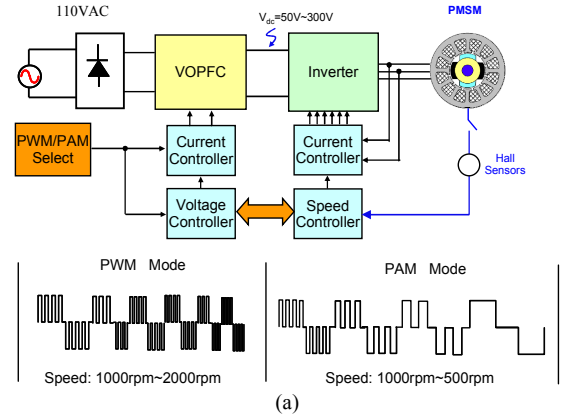


Fig. 12. The hysteresis comparison look-up table.

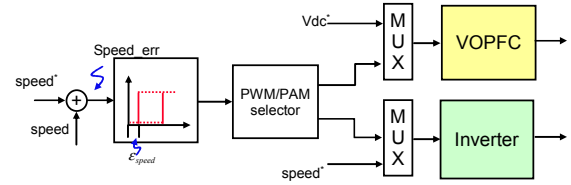


Fig. 13. The mode selection controller for PWM or PAM.

V. SIMULATION AND EXPERIMENTAL RESULTS

The proposed digital control strategy is verified through the simulation and experiment. The experiment has been realized with a DSP controlled BLDC motor drive. A switch-mode controller is designed to ensure the VOPFC converter working stability in buck mode or boost mode.

In Fig. 14(a), the output voltage is 100V, output power is 200W, and the ripple of output voltage is limited to 10%. In Fig. 14(b) and Fig. 15, the experiment waveforms verify that the VOPFC converter works well and regulates the constant output voltage in each buck mode or boost mode. The measured power factor is 94% and the efficiency is 93%. In Fig. 16, the motor can be operated stability in different dc voltage and the VOPFC can also be operation steady under the speed changing in simulation. The rated power and rated

speed of BLDC motor utilized in the present experiment are 550W and 3000rpm. With motor speed set at 1000rpm and having consistent torque load, the motor is operated independently under 100V bus voltage, with 20 kHz or 10 kHz switching frequency for each. The phase current I_a of the motor and the command signal K_d used to change operation switching frequency are shown in Fig. 17. When the system is operating alternately at 100V and 300V bus voltage, the switching loss in 100V voltage can reduce half of the one in 300V voltage for the same speed of motor. The efficiency of BLDCM drive can improve about 3%.

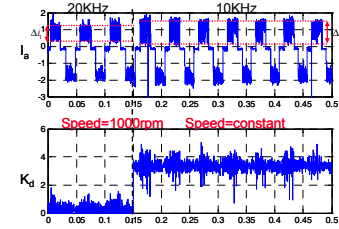


Fig. 17. The phase current I_a of the motor and the command signal K_d used to change operation switching frequency in experiment.

VI. CONCLUSION

This paper has proposed a dual-mode control strategy for BLDC motor drivers with power factor correction used in high-efficiency compressor applications. The output inverter stage can be operated in PAM mode or PWM mode with reduced switching frequency for efficiency optimization of the compressor motor drive to maintain a constant V/Hz ratio with specified current ripples. The proposed control scheme has been verified with a DSP-controlled VOPFC inverter motor driver and an efficiency improvement of 3% has been achieved. When the compressor drive runs in constant speed mode, the VOPFC converter can maintain a constant dc output with low input current THD during the transition between buck and boost modes. If the compressor driver runs in acceleration/deceleration mode, the dc-link voltage is controlled with a specified ramping rate. Based on the proposed control scheme, innovative PWM control schemes can be developed to improve the inverter efficiency and reduce the motor audio noise by controlling the PWM duties to achieve specified phase current profile.

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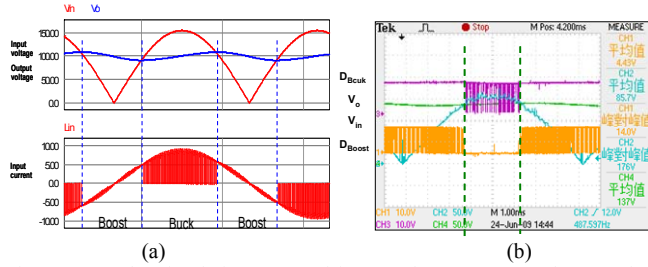


Fig. 14. (a) The simulation wave of input voltage, output voltage and the response input current. (b) The experiment wave of input voltage, output voltage and the buck and boost switching signals.

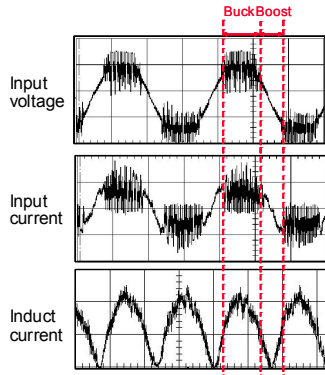


Fig. 15. The experiment waveforms of the input voltage, the input current, and the inductor current of the VOPFC converter when V_o is 100 V and P_o is 250 W.

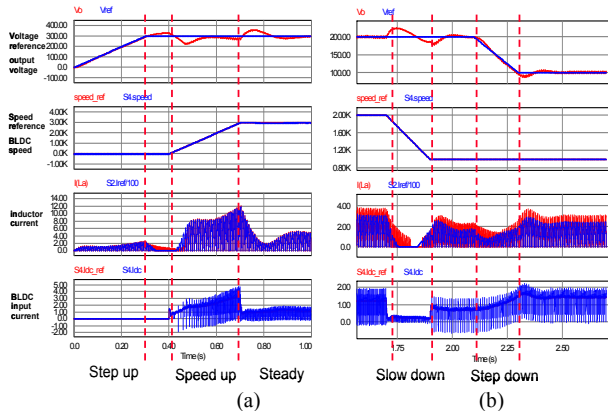


Fig. 16. (a) The VOPFC output voltage steady in variable speed control in simulation. (b) The motor speed response is stable in variable output voltage of VOPFC in simulation.

無衍生研發成果推廣資料

98 年度專題研究計畫研究成果彙整表

計畫主持人：鄒應嶼			計畫編號：98-2221-E-009-181-				
計畫名稱：高階伺服器電源系統數位控制架構之研究							
成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	1	1	100%		
		研討會論文	2	2	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	2	2	100%	人次	
		博士生	1	1	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	2	2	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無
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	成果項目	量化	名稱或內容性質簡述
科 教 處 計 畫 加 填 項 目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

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☒ 達成目標

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☐ 實驗失敗

☐ 因故實驗中斷

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說明：

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以本計畫之研究為基礎，目前已提出數位式 PFC 控制 IC 研製的產學計畫構想，並已與廠商進行討論，擬共同提出前瞻性之產學合作計畫。